XIAMEN OCULAR

GDC12864Z-FSY-FBW

SPECIFICATIONS OF LCD MODULE

1. General Specification

Interface With Parallel MPU

Driving IC: ST7565P

Display Dot Matrix: 128*64

Display Mode: Positive/Transflective/FSTN Type

Viewing Angle: 6 O'Clock

Display Duty: 1/64, Driving Bias: 1/9, LCD Driving Voltage: 9.8V

Power Supply: +3.3V DC

LED Backlight: Sidelight, Yellow-green Color, V_F=4.2V and I_F=60mA

Mechanical Characteristics (Unit: mm)

External Dimension: 72.0*46.0*6.5

View Area: 66.0*32.7

Dots Size: 0.45*0.45

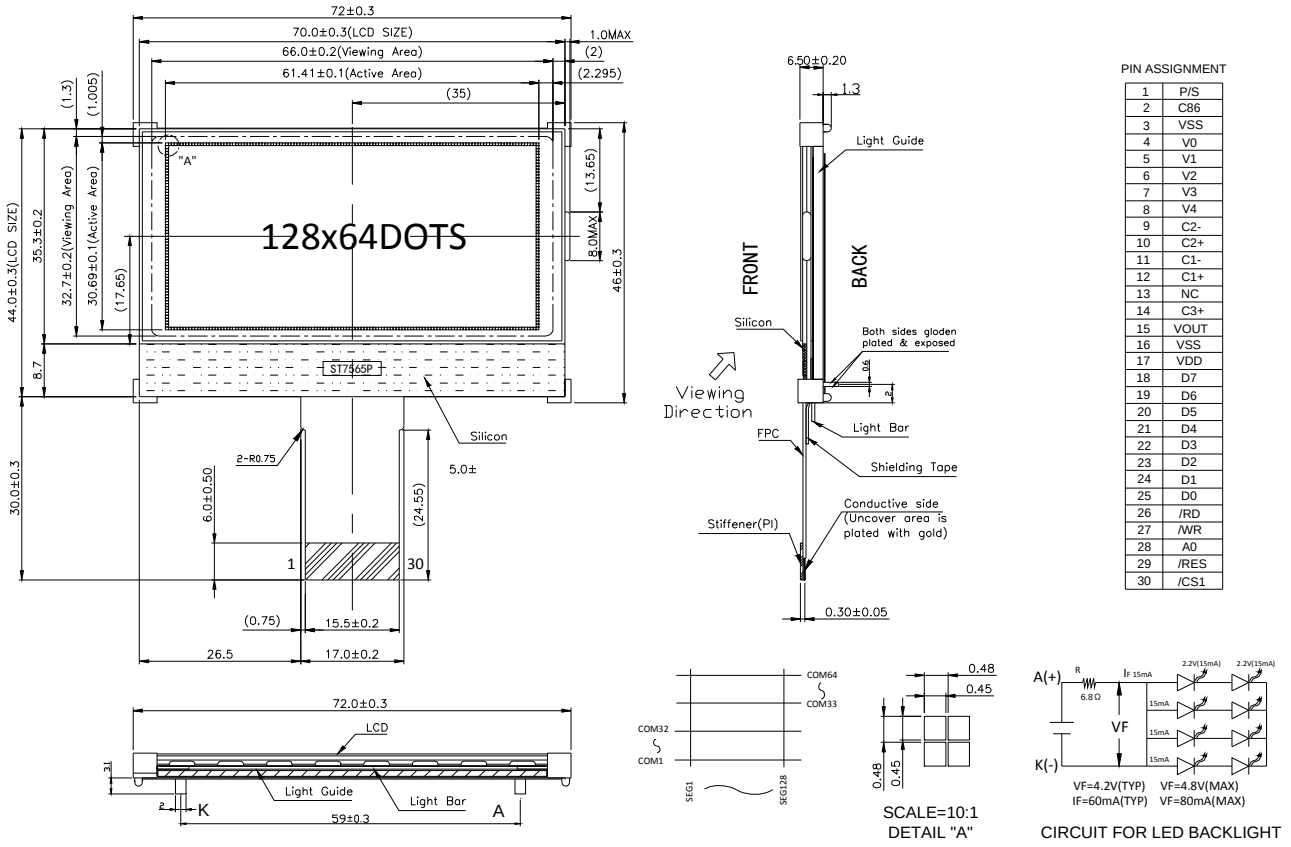
Dots Pitch: 0.48*0.48

Temperature Range

Operation Temperature: -20℃～70℃

Storage Temperature:-30℃～80℃

External Dimension



PIN ASSIGNMENT

1	P/S
2	C86
3	VSS
4	V0
5	V1
6	V2
7	V3
8	V4
9	C2-
10	C2+
11	C1-
12	C1+
13	NC
14	C3+
15	VOUT
16	VSS
17	VDD
18	D7
19	D6
20	D5
21	D4
22	D3
23	D2
24	D1
25	D0
26	/RD
27	/WR
28	A0
29	/RES
30	/CS1

PIN Assignment

<table>
<tr><th>Pin No</th><th>Symbol</th><th>I/O</th><th>Function</th></tr>
<tr><td>1</td><td>P/S</td><td>I</td><td>P/S=“H” :Parallel data input, P/S=“L” :serial data input</td></tr>
<tr><td>2</td><td>C86</td><td>I</td><td>C86=“H” :6800 series MPU interface
C86=“L” :8080 series MPU interface</td></tr>
<tr><td>3</td><td>VSS</td><td rowspan="6">Power Supply</td><td>Ground</td></tr>
<tr><td>4</td><td>V0</td><td rowspan="5">LCD driver supply voltage. The voltage determined by LCD cell is impedance-converted by a resistive driver or an operation amplifier for application .Voltages should be the following relationship:
V0>V1>V2>V3>V4>VSS
When the on-chip operating power circuit is on, the following are given to V1 to V4 by the on-chip power circuit .Voltage selection is performed by the set LCD bias command.
<table>
<tr><th>LCD BIAS</th><th>V1</th><th>V2</th><th>V3</th><th>V4</th></tr>
<tr><td>1/5BIAS</td><td>4/5V0</td><td>3/5V0</td><td>2/5V0</td><td>1/5V0</td></tr>
<tr><td>1/6 BIAS</td><td>5/6V0</td><td>4/6 V0</td><td>2/6 V0</td><td>1/6 V0</td></tr>
<tr><td>1/7 BIAS</td><td>6/7 V0</td><td>5/7 V0</td><td>2/7 V0</td><td>1/7 V0</td></tr>
<tr><td>1/8 BIAS</td><td>7/8 V0</td><td>6/8 V0</td><td>2/8 V0</td><td>1/8 V0</td></tr>
<tr><td>1/9 BIAS</td><td>8/9 V0</td><td>7/9 V0</td><td>2/9 V0</td><td>1/9 V0</td></tr>
</table></td></tr>
<tr><td>5</td><td>V1</td></tr>
<tr><td>6</td><td>V2</td></tr>
<tr><td>7</td><td>V3</td></tr>
<tr><td>8</td><td>V4</td></tr>
</table>

9	C2-	O	Capacitor2- for internal DC/DC voltage converter
10	C2+	O	Capacitor2+ for internal DC/DC voltage converter
11	C1-	O	Capacitor1- for internal DC/DC voltage converter
12	C1+	O	Capacitor1+ for internal DC/DC voltage converter
13	NC	O	
14	C3+	O	Capacitor3+ for internal DC/DC voltage converter
15	VOUT	O	DC/DC voltage converter output
16	VSS	Power Supply	Ground
17	VDD		Power supply for logic
18	D7	I/O	This is an 8-bit bi-directional data bus that connects to an 8-bit or 16-bit standard MPU data bus. When the serial interface is selected, then D7 serves as the serial data input terminal and D6 serves as the serial clock input terminal. At this time,D0-D5 are set to high impedance. When the chip select is inactive,D0 to D7 are set to high impedance.
19	D6		
20	D5		
21	D4		
22	D3		
23	D2		
24	D1		
25	D0		
26	/RD(E)	I	Operation (data read/write) enable signal.
27	/R/W	I	Read/write select signal.
28	A0	I	A0 = “H”: Indicates that D0 to D7 are display data. A0 = “L”: Indicates that D0 to D7 are control data.
29	RST	I	When RST is set to “L” ,the setting are initialized The RST operation is performed by the RST signal level
30	CS1B	I	This is the chip select signal .When CS1B=“L” and CS2B=“H”, then the chip select becomes active, and data/command I/O is enabled

Backlight

Optical Electronic Characteristics

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
Forward Voltage	V_F	Ta= 25℃, I_F=60mA	-	4.2	-	V
Luminous	_		100	_	_	Cd/m^2

Absolute Maximum Ratings

Item	Symbol	Condition	Min	Max	Unit
Power supply voltage	V_{DD}		0.3	+5.0	V
Input voltage	Vin		-0.3	V_{DD}+0.3	V
DC Supply Voltage	V_0,V_{OUT}		0.3	+18.0	V
Operating temperature	T_{OP}		-20	70	℃
Storage temperature	T_{ST}		-30	80	℃

Electrical Characteristics

Item	Symbol	Condition	Min	Typ	Max	Unit
Power supply voltage	V_{DD}		1.8	-	3.3	V
Current consumption	I_{DD}	Ta=25℃	-	1.0	-	mA

DC Characteristics

Unless otherwise specified, Vss = 0 V, VDD = 3.0 V ± 10%, Ta = –40 to 85°C

Table 18

Item		Symbol	Condition		Rating Min.	Rating Typ.	Rating Max.	Units	Applicable Pin
Operating Voltage (1)		VDD			1.8	—	3.3	V	Vss*1
Operating Voltage (2)		VDD2	(Relative to Vss)		2.4	—	3.3	V	Vss
High-level Input Voltage		VIHC			0.8 x VDD	—	VDD	V	*3
Low-level Input Voltage		VILC			Vss	—	0.2 x VDD	V	*3
High-level Output Voltage		VOHC	IOH = –0.5 mA		0.8 x VDD	—	VDD	V	*4
Low-level Output Voltage		VOLC	IOL = 0.5 mA		Vss	—	0.2 x VDD	V	*4
Input leakage current		ILI	VIN = VDD or Vss		–1.0	—	1.0	μA	*5
Output leakage current		ILO	VIN = VDD or Vss		–3.0	—	3.0	μA	*6
Liquid Crystal Driver ON Resistance		RON	Ta = 25°C (Relative To VDD)	V0 = 13.0 V	—	2.0	3.5	KΩ	SEGn COMn *7
				V0 = 8.0 V	—	3.2	5.4		
Static Consumption Current		ISSQ	V0 = 13.0 V(Relative To VDD)		—	0.01	2	μA	VDD, VDD2
Output Leakage Current		ISQ			—	0.01	10	μA	V0
Input Terminal Capacitance		CIN	Ta = 25°C , f = 1 MHz		—	5.0	8.0	pF	
Oscillator Frequency	Internal Oscillator	fOSC	1/65 duty 1/33 duty	Ta = 25°C	17	20	24	kHz	*8
	External Input	fCL			17	20	24	kHz	CL
	Internal Oscillator	fOSC	1/49 duty 1/53 duty 1/55 duty	Ta = 25°C	25	30	35	kHz	*8
	External Input	fCL			25	30	35	kHz	CL

Timing Characteristics

System bus read/write characteristics 1 (8080 Series MPU)

System Bus Read/Write Characteristics 1 (For the 8080 Series MPU)

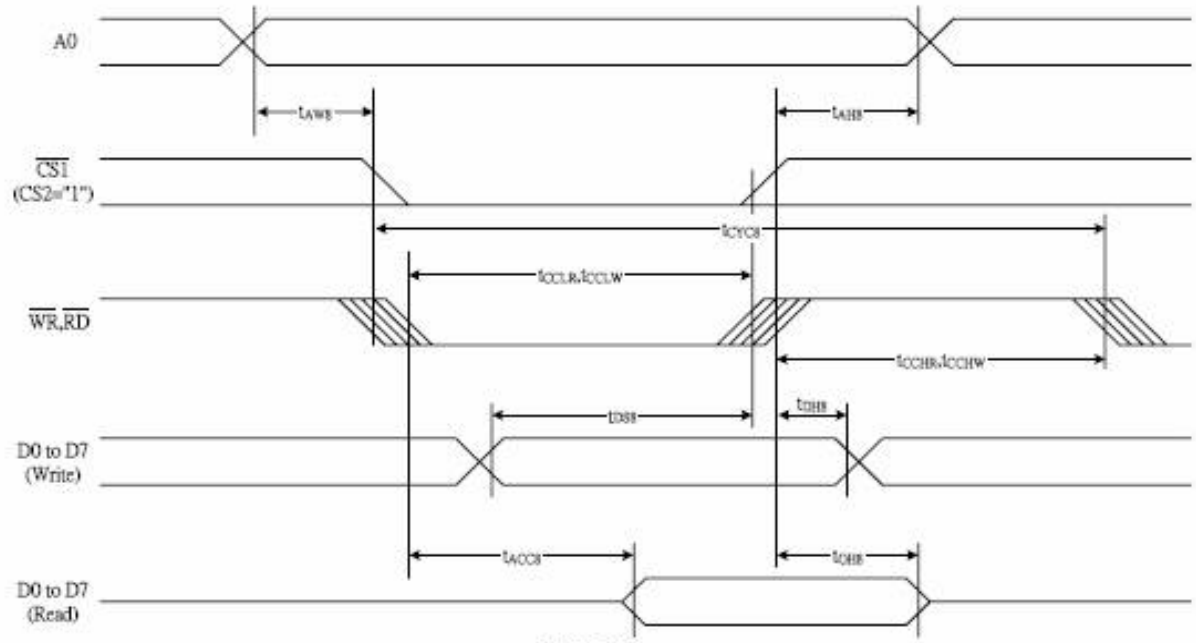


Figure 37

Table 24

(VDD = 3.3V , Ta =25°C)

Item	Signal	Symbol	Condition	Rating		Units
				Min.	Max.	
Address hold time	A0	tAH8		0	—	Ns
Address setup time		tAW8		0	—	
System cycle time		tCYC8		240	—	
Enable L pulse width (WRITE)	WR	tCCLW		80	—	
Enable H pulse width (WRITE)		tCCHW		80	—	
Enable L pulse width (READ)	RD	tCCLR		140	—	
Enable H pulse width (READ)		tCCHR		80		
WRITE Data setup time	D0 to D7	tDS8		40	—	
WRITE Address hold time		tDH8		0	—	
READ access time		tACC8	CL = 100 pF	—	70	
READ Output disable time		tOH8	CL = 100 pF	5	50	

(V_{DD} = 2.7 V , Ta = 25°C)

Item	Signal	Symbol	Condition	Rating		Units
				Min.	Max.	
Address hold time	A0	t_{AH8}		0	—	ns
Address setup time		t_{AW8}		0	—	
System cycle time		t_{CYC8}		400	—	
Enable L pulse width (WRITE)	WR	t_{CCLW}		220	—	
Enable H pulse width (WRITE)		t_{CCHW}		180	—	
Enable L pulse width (READ)	RD	t_{CCLR}		220	—	
Enable H pulse width (READ)		t_{CCHR}		180	—	
WRITE Data setup time	D0 to D7	t_{DS8}		40	—	
WRITE Address hold time		t_{DH8}		0	—	
READ access time		t_{ACC8}	C_L = 100 pF	—	140	
READ Output disable time		t_{OH8}	C_L = 100 pF	10	100	

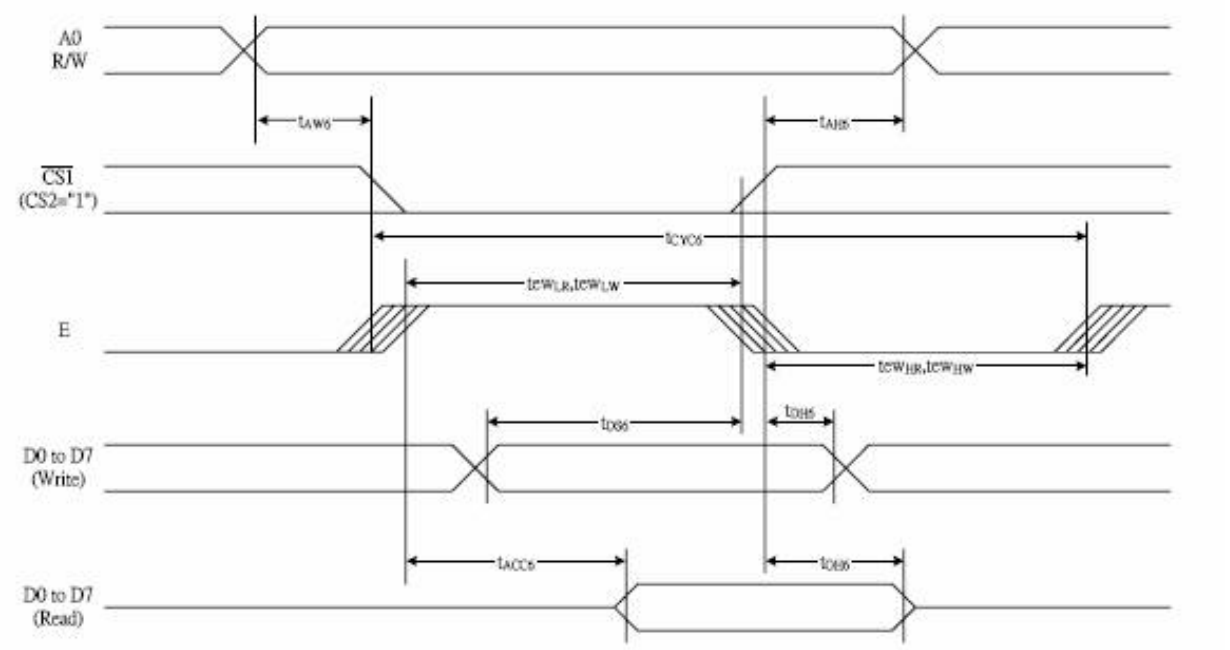
Table 26

(V_{DD} = 1.8V , Ta = 25°C)

Item	Signal	Symbol	Condition	Rating		Units
				Min.	Max.	
Address hold time	A0	t_{AH8}		0	—	ns
Address setup time		t_{AW8}		0	—	
System cycle time		t_{CYC8}		640	—	
Enable L pulse width (WRITE)	WR	t_{CCLW}		360	—	
Enable H pulse width (WRITE)		t_{CCHW}		280	—	
Enable L pulse width (READ)	RD	t_{CCLR}		360	—	
Enable H pulse width (READ)		t_{CCHR}		280		
WRITE Data setup time	D0 to D7	t_{DS8}		80	—	
WRITE Address hold time		t_{DH8}		0	—	
READ access time		t_{ACC8}	C_L = 100 pF	—	240	
READ Output disable time		t_{OH8}	C_L = 100 pF	10	200	

*1 The input signal rise time and fall time (t_r, t_f) is specified at 15 ns or less. When the system cycle time is extremely fast, ($t_r + t_f$) ≦ (t_{CYC8} – t_{CCLW} – t_{CCHW}) for ($t_r + t_f$) ≦ (t_{CYC8} – t_{CCLR} – t_{CCHR}) are specified.
*2 All timing is specified using 20% and 80% of V_{DD} as the reference.
*3 t_{CCLW} and t_{CCLR} are specified as the overlap between /CS1 being "L" (CS2 = "H") and /WR and /RD being at the "L" level.

System bus read/write characteristics 2 (6800 Series MPU)



(VDD = 3.3 V , Ta = 25°C)

Item	Signal	Symbol	Condition	Rating		Units
				Min.	Max.	
Address hold time	A0	tAH6		0	—	ns
Address setup time		tAW6		0	—	
System cycle time		tCYC6		240	—	
Enable L pulse width (WRITE)	WR	tEWLW		80	—	
Enable H pulse width (WRITE)		tEWHW		80	—	
Enable L pulse width (READ)	RD	tEWLR		80	—	
Enable H pulse width (READ)		tEWHR		140		
WRITE Data setup time	D0 to D7	tDS6		40	—	
WRITE Address hold time		tDH6		0	—	
READ access time		tACC6	CL = 100 pF	—	70	
READ Output disable time		tOH6	CL = 100 pF	5	50	

(V_{DD} = 2.7V , Ta =25°C)

Item	Signal	Symbol	Condition	Rating		Units
				Min.	Max.	
Address hold time	A0	t_{AH6}		0	—	ns
Address setup time		t_{AW6}		0	—	
System cycle time		t_{CYC6}		400	—	
Enable L pulse width (WRITE)	WR	t_{EWLW}		220	—	
Enable H pulse width (WRITE)		t_{EWHW}		180	—	
Enable L pulse width (READ)	RD	t_{EWLR}		220	—	
Enable H pulse width (READ)		t_{EWHR}		180	—	
WRITE Data setup time	D0 to D7	t_{DS6}		40	—	
WRITE Address hold time		t_{DH6}		0	—	
READ access time		t_{ACC6}	C_L = 100 pF	—	140	
READ Output disable time		t_{OH6}	C_L = 100 pF	10	100	

Table 29

(V_{DD} =1.8V , Ta =25°C)

Item	Signal	Symbol	Condition	Rating		Units
				Min.	Max.	
Address hold time	A0	t_{AH6}		0	—	ns
Address setup time		t_{AW6}		0	—	
System cycle time		t_{CYC6}		640	—	
Enable L pulse width (WRITE)	WR	t_{EWLW}		360	—	
Enable H pulse width (WRITE)		t_{EWHW}		280	—	
Enable L pulse width (READ)	RD	t_{EWLR}		360	—	
Enable H pulse width (READ)		t_{EWHR}		280	—	
WRITE Data setup time	D0 to D7	t_{DS6}		80	—	
WRITE Address hold time		t_{DH6}		0	—	
READ access time		t_{ACC6}	C_L = 100 pF	—	240	
READ Output disable time		t_{OH6}	C_L = 100 pF	10	200	

*1 The input signal rise time and fall time (t_r, t_f) is specified at 15 ns or less. When the system cycle time is extremely fast, ($t_r + t_f$) ≦ ($t_{CYC6} - t_{EWLW} - t_{EWHW}$) for ($t_r + t_f$) ≦ ($t_{CYC6} - t_{EWLR} - t_{EWHR}$) are specified.
*2 All timing is specified using 20% and 80% of V_{DD} as the reference.
*3 t_{EWLW} and t_{EWLR} are specified as the overlap between $\overline{CS1}$ being "L" (CS2 = "H") and E.

IC Specification

The ST7565R identify the data bus signals by a combination of A0, /RD (E), /WR(R/W) signals. Command interpretation and execution does not depend on the external clock, but rather is performed through internal timing only, and thus the processing is fast enough that normally a busy check is not required.

In the 8080 MPU interface, commands are launched by inputting a low pulse to the RD terminal for reading, and inputting a low pulse to the /WR terminal for writing. In the 6800 Series MPU interface, the interface is placed in a read mode when an "H" signal is input to the R/W terminal and placed in a write mode when a "L" signal is input to the R/W terminal and then the command is launched by inputting a high pulse to the E terminal. Consequently, the 6800 Series MPU interface is different than the 80x86 Series MPU interface in that

in the explanation of commands and the display commands the status read and display data read /RD (E) becomes “1(H)”. In the explanations below the commands are explained using the 8080 Series MPU interface as the example.

When the serial interface is selected, the data is input in sequence starting with D7.

Instruction Table

Command	Command Code										Function
	A0	/RD	/WR	D7	D6	D5	D4	D3	D2	D1	D0	
(1) Display ON/OFF	0	1	0	1	0	1	0	1	1	1	0 1	LCD display ON/OFF 0: OFF, 1: ON
(2) Display start line set	0	1	0	0	1	Display start address						Sets the display RAM display start line address
(3) Page address set	0	1	0	1	0	1	1	Page address				Sets the display RAM page address
(4) Column address set upper bit Column address set lower bit	0 0	1 1	0 0	0 0	0 0	0 0	1 0	Most significant column address Least significant column address				Sets the most significant 4 bits of the display RAM column address. Sets the least significant 4 bits of the display RAM column address.
(5) Status read	0	0	1	Status				0	0	0	0	Reads the status data
(6) Display data write	1	1	0	Write data								Writes to the display RAM
(7) Display data read	1	0	1	Read data								Reads from the display RAM
(8) ADC select	0	1	0	1	0	1	0	0	0	0	0 1	Sets the display RAM address SEG output correspondence 0: normal, 1: reverse
(9) Display normal/ reverse	0	1	0	1	0	1	0	0	1	1	0 1	Sets the LCD display normal/ reverse 0: normal, 1: reverse
(10) Display all points ON/OFF	0	1	0	1	0	1	0	0	1	0	0 1	Display all points 0: normal display 1: all points ON
(11) LCD bias set	0	1	0	1	0	1	0	0	0	1	0 1	Sets the LCD drive voltage bias ratio 0: 1/9 bias, 1: 1/7 bias (ST7565P)
(12) Read/modify/write	0	1	0	1	1	1	0	0	0	0	0	Column address increment At write: +1 At read: 0
(13) End	0	1	0	1	1	1	0	1	1	1	0	Clear read/modify/write
(14) Reset	0	1	0	1	1	1	0	0	0	1	0	Internal reset
(15) Common output mode select	0	1	0	1	1	0	0	0 1	*	*	*	Select COM output scan direction 0: normal direction 1: reverse direction
(16) Power control set	0	1	0	0	0	1	0	1	Operating mode			Select internal power supply operating mode
(17) Vo voltage regulator internal resistor ratio set	0	1	0	0	0	1	0	0	Resistor ratio			Select internal resistor ratio(Rb/Ra) mode
(18) Electronic volume mode set Electronic volume register set	0	1	0	1 0	0 0	0 Electronic volume value	0	0	0	0	1	Set the Vo output voltage electronic volume register
(19) Static indicator ON/OFF Static indicator register set	0	1	0	1 0	0 0	1 0	0 0	1 0	1 0	0 0	0 1 Mode	0: OFF, 1: ON Set the flashing mode
(20) Booster ratio set	0	1	0	1 0	1 0	1 0	1 0	1 0	0 0	0 step-up value	0	select booster ratio 00: 2x,3x,4x 01: 5x 11: 6x
(21) Power saver												Display OFF and display all points ON compound command
(22) NOP	0	1	0	1	1	1	0	0	0	1	1	Command for non-operation
(23) Test	0	1	0	1	1	1	1	*	*	*	*	Command for IC test. Do not use this command

Instruction Description

1. Display ON/OFF

This command turns the display ON and OFF.

	E	R/W								
A0	/RD	/WR	D7	D6	D5	D4	D3	D2	D1	D0	Setting
0	1	0	1	0	1	0	1	1	1	1	Display ON
										0	Display OFF

When the display OFF command is executed when in the display all points ON mode, power saver mode is entered. See the section on the power saver for details.

2. Display Start Line Set

This command is used to specify the display start line address of the display data RAM shown in Figure 4. For further details see the explanation of this function in "The Line Address Circuit".

	E	R/W									
A0	/RD	/WR	D7	D6	D5	D4	D3	D2	D1	D0	Line address
0	1	0	0	1	0	0	0	0	0	0	0
					0	0	0	0	0	1	1
					0	0	0	0	1	0	2
							↓				↓
					1	1	1	1	1	0	62
					1	1	1	1	1	1	63

3. Page Address Set

This command specifies the page address corresponding to the low address when the MPU accesses the display data RAM (see Figure 4). Specifying the page address and column address enables to access a desired bit of the display data RAM. Changing the page address does not accompany a change in the status display.

	E	R/W								
A0	/RD	/WR	D7	D6	D5	D4	D3	D2	D1	D0	Page address
0	1	0	1	0	1	1	0	0	0	0	0
							0	0	0	1	1
							0	0	1	0	2
								↓			↓
							0	1	1	1	7
							1	0	0	0	8

4. Column Address

This command specifies the column address of the display data RAM shown in Figure 4. The column address is split into two sections (the higher 4 bits and the lower 4 bits) when it is set (fundamentally, set continuously). Each time the display data RAM is accessed, the column address automatically increments (+1), making it possible for the MPU to continuously read from/write to the display data. The column address increment is topped at 83H. This does not change the page address continuously. See the function explanation in "The Column Address Circuit," for details.

		E	R/W																
	A0	/RD	/WR	D7	D6	D5	D4	D3	D2	D1	D0	A7	A6	A5	A4	A3	A2	A1	A0	Column address
High bits →	0	1	0	0	0	0	1	A7	A6	A5	A4	0	0	0	0	0	0	0	0	0
Low bits →							0	A3	A2	A1	A0	0	0	0	0	0	0	0	1	1
												0	0	0	0	0	0	1	0	2
																↓				↓
												1	0	0	0	0	0	1	0	130
												1	0	0	0	0	0	1	1	131

5. Status Read

A0	E /RD	R/W /WR	D7	D6	D5	D4	D3	D2	D1	D0
0	0	1	BUSY	ADC	ON/OFF	RESET	0	0	0	0

BUSY	BUSY = 1: it indicates that either processing is occurring internally or a reset condition is in process. BUSY = 0: A new command can be accepted . if the cycle time can be satisfied, there is no need to check for BUSY conditions.
ADC	This shows the relationship between the column address and the segment driver. 0: Normal (column address n ↔ SEG n) 1: Reverse (column address 131-n ↔ SEG n) (The ADC command switches the polarity.)
ON/OFF	ON/OFF: indicates the display ON/OFF state. 0: Display ON 1: Display OFF (This display ON/OFF command switches the polarity.)
RESET	This indicates that the chip is in the process of initialization either because of a /RES signal or because of a reset command. 0: Operating state 1: Reset in progress

6. Display Data Write

This command writes 8-bit data to the specified display data RAM address. Since the column address is automatically incremented by "1" after the write, the MPU can write the display data.

A0	E /RD	R/W /WR	D7 D6 D5 D4 D3 D2 D1 D0
1	1	0	Write data

7. Display Data Read

This command reads 8-bit data from the specified display data RAM address. Since the column address is automatically incremented by "1" after the read, the CPU can continuously read multiple-word data. One dummy read is required immediately after the column address has been set. See the function explanation in "Display Data RAM" for the explanation of accessing the internal registers. When the serial interface is used, reading of the display data becomes unavailable.

A0	E /RD	R/W /WR	D7 D6 D5 D4 D3 D2 D1 D0
1	0	1	Read data

8. ADC Select (Segment Driver Direction Select)

This command can reverse the correspondence between the display RAM data column address and the segment driver output. Thus, sequence of the segment driver output pins may be reversed by the command. See the column address circuit for the detail. Increment of the column address (by "1") accompanying the reading or writing the display data is done according to the column address indicated in Figure 4.

A0	E /RD	R/W /WR	D7	D6	D5	D4	D3	D2	D1	D0	Setting
0	1	0	1	0	1	0	0	0	0	0	Normal
										1	Reverse

9. Display Normal/Reverse

This command can reverse the lit and unlit display without overwriting the contents of the display data RAM. When this is done the display data RAM contents are maintained.

	E	R/W								
A0	/RD	/WR	D7	D6	D5	D4	D3	D2	D1	D0	Setting
0	1	0	1	0	1	0	0	1	1	0	RAM Data "H" LCD ON voltage (normal)
										1	RAM Data "L" LCD ON voltage (reverse)

10. Display All Points ON/OFF

This command makes it possible to force all display points ON regardless of the content of the display data RAM. The contents of the display data RAM are maintained when this is done. This command takes priority over the display normal/reverse command.

	E	R/W								
A0	/RD	/WR	D7	D6	D5	D4	D3	D2	D1	D0	Setting
0	1	0	1	0	1	0	0	1	0	0	Normal display mode
										1	Display all points ON

When the display is in an OFF mode, executing the display all points ON command will place the display in power save mode. For details, see the Power Save section.

11. LCD Bias Set

This command selects the voltage bias ratio required for the liquid crystal display.

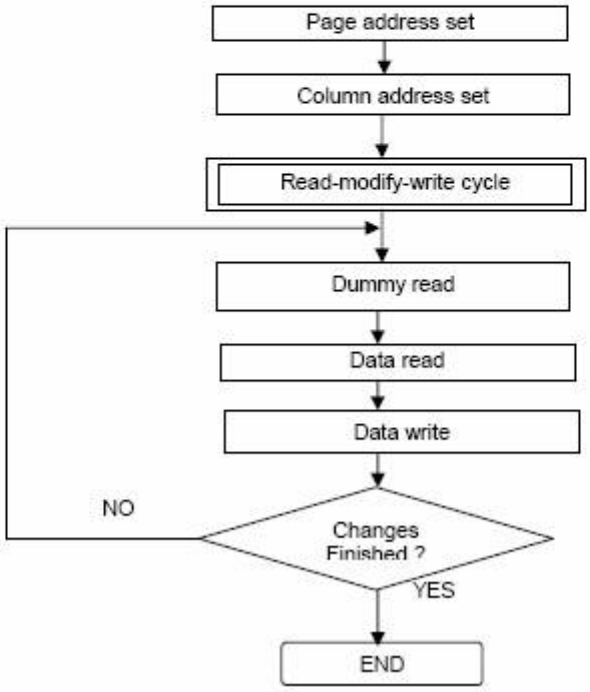
	E	R/W								Select Status				
A0	/RD	/WR	D7	D6	D5	D4	D3	D2	D1	D0	1/65duty	1/49duty	1/33duty	1/55duty	1/53duty
0	1	0	1	0	1	0	0	0	1	0	1/9 bias	1/8 bias	1/6 bias	1/8 bias	1/8 bias
										1	1/7 bias	1/6 bias	1/5 bias	1/6 bias	1/6 bias

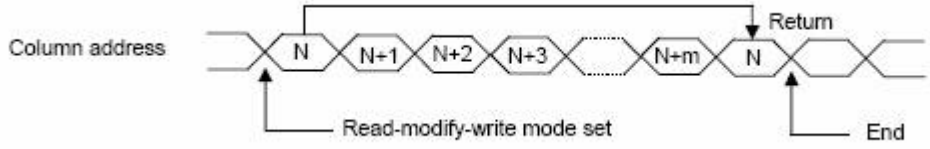
12. Read/Modify/Write

This command is used paired with the "END" command. Once this command has been input, the display data read command does not change the column address, but only the display data write command increments (+1) the column address. This mode is maintained until the END command is input. When the END command is input, the column address returns to the address it was at when the read/modify/write command was entered. This function makes it possible to reduce the load on the MPU when there are repeating data changes in a specified display region, such as when there is a blanking cursor.

	E	R/W							
A0	/RD	/WR	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	1	1	1	0	0	0	0	0

* Even in read/modify/write mode, other commands aside from display data read/write commands can also be used.





13. End

This command releases the read/modify/write mode, and returns the column address to the address it was at when the mode was entered.

	E	R/W							
A0	/RD	/WR	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	1	1	1	0	1	1	1	0

14. Reset

This command initializes the display start line, the column address, the page address, the common output mode, the Vo voltage regulator internal resistor ratio, the electronic volume, and the static indicator are reset, and the read/modify/write mode and test mode are released. There is no impact on the display data RAM. See the function explanation in "Reset" for details.
The reset operation is performed after the reset command is entered.

A0	E /RD	R/W /WR	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	1	1	1	0	0	0	1	0

The initialization when the power supply is applied must be done through applying a reset signal to the /RES terminal. The reset command must not be used instead.

15. Common Output Mode Select

This command can select the scan direction of the COM output terminal. For details, see the function explanation in "Common Output Mode Select Circuit."

A0	E /RD	R/W /WR	D7	D6	D5	D4	D3	D2	D1	D0	Selected Mode	1/65duty	1/49duty	1/33duty	1/55duty	1/53duty
0	1	0	1	1	0	0	0	*	*	*	Normal	COM0→COM63	COM0→COM47	COM0→COM31	COM0→COM53	COM0→COM51
							1				Reverse	COM63→COM0	COM47→COM0	COM31→COM0	COM53→COM0	COM51→COM0

* Disabled bit

16. Power Controller Set

This command sets the power supply circuit functions. See the function explanation in "The Power Supply Circuit," for details

A0	E /RD	R/W /WR	D7	D6	D5	D4	D3	D2	D1	D0	Selected Mode
0	1	0	0	0	1	0	1	0			Booster circuit: OFF
								1			Booster circuit: ON
									0		Voltage regulator circuit: OFF
									1		Voltage regulator circuit: ON
										0	Voltage follower circuit: OFF
										1	Voltage follower circuit: ON

17. V0 Voltage Regulator Internal Resistor Ratio Set

This command sets the Vo voltage regulator internal resistor ratio. For details, see the function explanation is "The Voltage Regulator circuit " and table 11 .

A0	E /RD	R/W /WR	D7	D6	D5	D4	D3	D2	D1	D0	Rb/Ra Ratio
0	1	0	0	0	1	0	0	0	0	0	Small
								0	0	1	
								0	1	0	
									↓		↓
								1	1	1	
								1	1	1	Large

18. The Electronic Volume (Double Byte Command)

This command makes it possible to adjust the brightness of the liquid crystal display by controlling the LCD drive voltage V0 through the output from the voltage regulator circuits of the internal liquid crystal power supply. This command is a two byte command used as a pair with the electronic volume mode set command and the electronic volume register set command, and both commands must be issued one after the other.

19. The Electronic Volume Mode Set

When this command is input, the electronic volume register set command becomes enabled. Once the electronic volume mode has been set, no other command except for the electronic volume register command can be used. Once the electronic volume register set command has been used to set data into the register, then the electronic volume mode is released.

	E	R/W							
A0	/RD	/WR	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	1	0	0	0	0	0	0	1

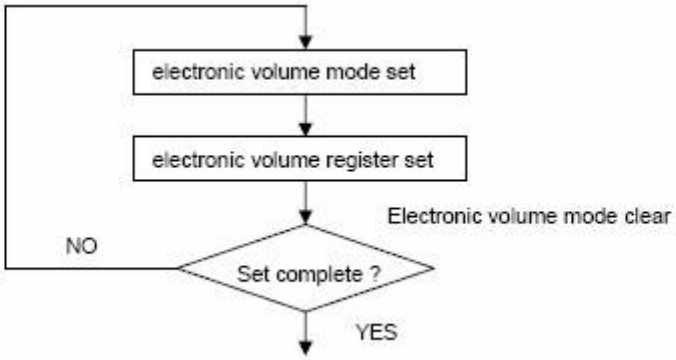
20. Electronic Volume Register Set

By using this command to set six bits of data to the electronic volume register, the liquid crystal drive voltage V0 assumes one of the 64 voltage levels.
When this command is input, the electronic volume mode is released after the electronic volume register has been set.

	E	R/W								
A0	/RD	/WR	D7	D6	D5	D4	D3	D2	D1	D0	| V0 |
0	1	0	*	*	0	0	0	0	0	1	Small
			*	*	0	0	0	0	1	0	
			*	*	0	0	0	0	1	1	
							↓				↓
			*	*	1	1	1	1	1	0	
			*	*	1	1	1	1	1	1	Large

* Inactive bit (set "0")
When the electronic volume function is not used, set this to (1, 0, 0, 0, 0, 0)

21. The Electronic Volume Register Set Sequence



22. Static Indicator (Double Byte Command)

This command controls the static drive system indicator display. The static indicator display is controlled by this command only, and is independent of other display control commands.
This is used when one of the static indicator liquid crystal drive electrodes is connected to the FR terminal, and the other is connected to the FRS terminal. A different pattern is recommended for the static indicator electrodes than for the dynamic drive electrodes. If the pattern is too close, it can result in deterioration of the liquid crystal and of the electrodes.
The static indicator ON command is a double byte command paired with the static indicator register set command, and thus one must execute one after the other. (The static indicator OFF command is a single byte command.)

23. Static Indicator ON/OFF

When the static indicator ON command is entered, the static indicator register set command is enabled. Once the static indicator ON command has been entered, no other command aside from the static indicator register set command can be used. This mode is cleared when data is set in the register by the static indicator register set command.

A0	E /RD	R/W /WR	D7	D6	D5	D4	D3	D2	D1	D0	Static Indicator
0	1	0	1	0	1	0	1	1	0	0	OFF
										1	ON

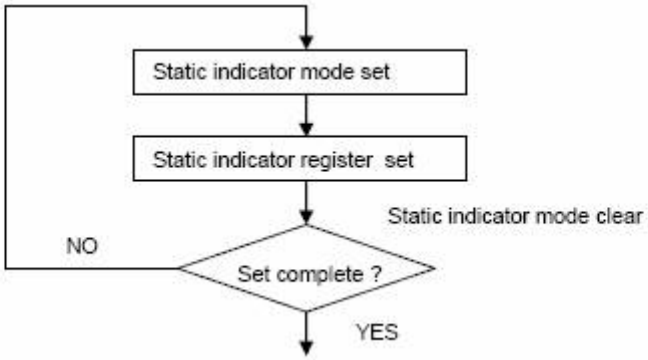
24. Static Indicator Register Set

This command sets two bits of data into the static indicator register, and is used to set the static indicator into a blinking mode.

A0	E /RD	R/W /WR	D7	D6	D5	D4	D3	D2	D1	D0	Indicator Display State
0	1	0	*	*	*	*	*	*	0	0	OFF
									0	1	ON (blinking at approximately one second intervals)
									1	0	ON (blinking at approximately 0.5 second intervals)
									1	1	ON (constantly on)

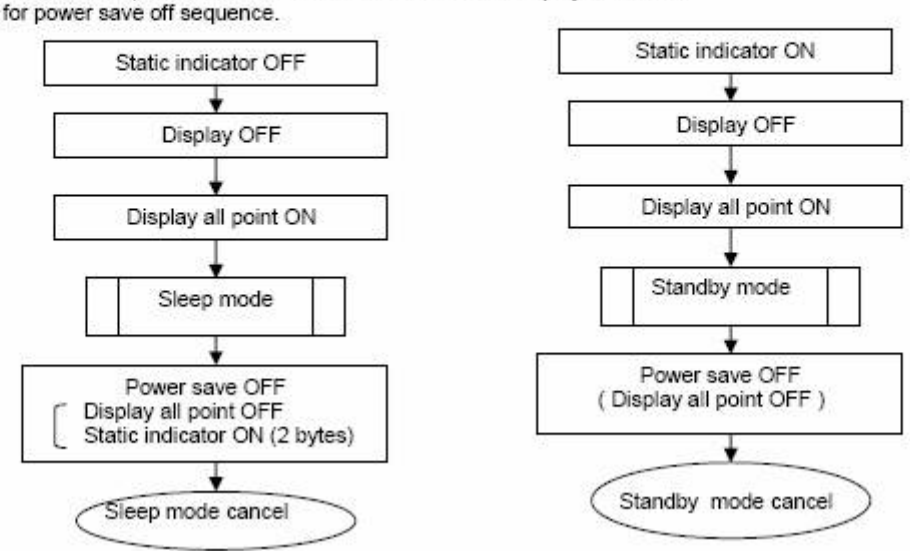
* Disabled bit (set "0")

25. Static Indicator Register Set Sequence



26. Power Save (Compound Command)

When the display all points ON is performed while the display is in the OFF mode, the power saver mode is entered, thus greatly reducing power consumption.
The power saver mode has two different modes: the sleep mode and the standby mode. When the static indicator is OFF, it is the sleep mode that is entered. When the static indicator is ON, it is the standby mode that is entered.
In the sleep mode and in the standby mode, the display data is saved as is the operating mode that was in effect before the power saver mode was initiated, and the MPU is still able to access the display data RAM.
Refer to figure 28 for power save off sequence.



27. Sleep Mode

This stops all operations in the LCD display system, and as long as there are no accesses from the MPU, the consumption current is reduced to a value near the static current. The internal modes during sleep mode are as follows:
1. The oscillator circuit and the LCD power supply circuit are halted.
2. All liquid crystal drive circuits are halted, and the segment in common drive outputs output a Vss level.

28. Standby Mode

The duty LCD display system operations are halted and only the static drive system for the indicator continues to operate, providing the minimum required consumption current for the static drive. The internal modes are in the following states during standby mode.
1 The LCD power supply circuits are halted. The oscillator circuit continues to operate.
2 The duty drive system liquid crystal drive circuits are halted and the segment and common driver outputs output a Vss level. The static drive system does not operate.
When a reset command is performed while in standby mode, the system enters sleep mode.
* When an external power supply is used, it is recommended that the functions of the external power supply circuit be stopped when the power saver mode is started. For example, when the various levels of liquid crystal drive voltage are provided by external resistive voltage dividers, it is recommended that a circuit be added in order to cut the electrical current flowing through the resistive voltage divider circuit when the power saver mode is in effect. The ST7565P series chips have a liquid crystal display blanking control terminal /DOF. This terminal enters an "L" state when the power saver mode is launched. Using the output of /DOF, it is possible to stop the function of an external power supply circuit.
* When the master is turned on, the oscillator circuit is operable immediately after the powering on.

29. The Booster Ratio (Double Byte Command)

This command makes it possible to select step-up ratio. It is used when the power control set have turn on the internal booster circuit. This command is a two byte command used as a pair with the booster ratio select mode set command and the booster ratio register set command, and both commands must be issued one after the other.

30. Booster Ratio Select Mode Set

This command makes it possible to select step-up ratio. It is used when the power control set have turn on the internal booster circuit. This command is a two byte command used as a pair with the booster ratio select mode set command and the booster ratio register set command, and both commands must be issued one after the other.

Booster Ratio Select Mode Set

When this command is input, the Booster ratio register set command becomes enabled. Once the booster ratio select mode has been set, no other command except for the booster ratio register command can be used. Once the booster ratio register set command has been used to set data into the register, then the booster ratio select mode is released.

	E	R/W							
A0	/RD	/WR	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	1	1	1	1	1	0	0	0

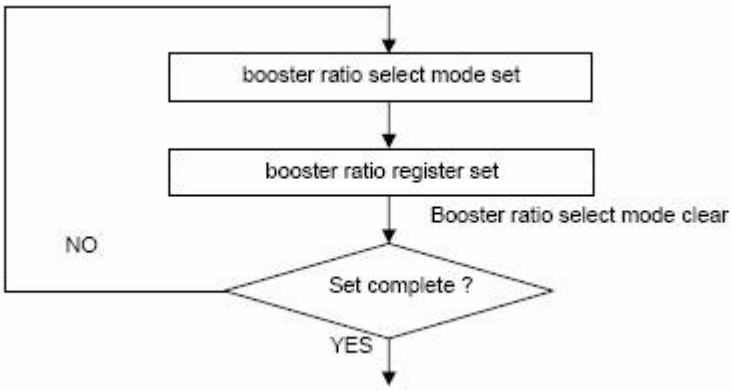
31. Booset Ratio Register Set

By using this command to set two bits of data to the booster ratio register, it can be select what kind of the booster ratio can be used.
When this command is input, the booster ratio select mode is released after the booster ratio register has been set.

	E	R/W								
A0	/RD	/WR	D7	D6	D5	D4	D3	D2	D1	D0	Booster ratio select
0	1	0	*	*	*	*	*	*	0	0	2x,3x,4x
			*	*	*	*	*	*	0	1	5x
			*	*	*	*	*	*	1	1	6x

* Inactive bit (set "0")
When the booster ratio select function is not used, set this to (0, 0) 2x,3x,4x step-up mode

32. The booster ratio Register Set Sequence



33. NOP

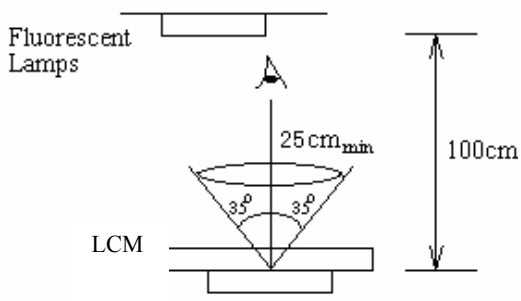
Non-Operation Command

	E	R/W							
A0	/RD	/WR	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	1	1	1	0	0	0	1	1

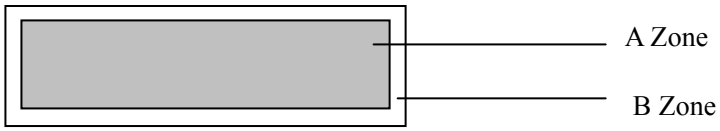
Quality Specifications

Cosmetic Inspection

The inspection should be performed in using 20W x 2 fluorescent lamps. Distance between LCM and fluorescent lamps should be 100 cm or more. Distance between LCM and inspector eyes should be 25 cm or more. Viewing direction for inspection is 35° from vertical against LCM.



Definition of zone:



A Zone: Active display area (minimum viewing area).

B Zone: Non-active display area (outside viewing area).

AQL Level

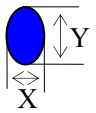
Sampling method: MIL-STD-105E, Level II, normal one time sampling

Defect classification

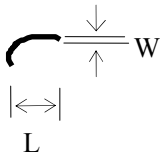
Classify	Item		Note	AQL
Major	Display state	Short or open circuit	1	0.65
		LC leakage		
		Flickering		
		No display		
		Wrong viewing direction		
		Contrast defect (dim, ghost)	2	
		Back-light	1,8	
	Non-display	Flat cable or pin reverse	10	
		Wrong or missing component	11	
Minor	Display state	Background color deviation	2	1.0
		Black spot and dust	3	
		Line defect, Scratch	4	
		Rainbow	5	
		Chip	6	
		Pin hole	7	
	Polarizer	Protruded	12	
		Bubble and foreign material	3	
	Soldering	Poor connection	9	
	Wire	Poor connection	10	
	TAB	Position, Bonding strength	13	

Note on defect classification

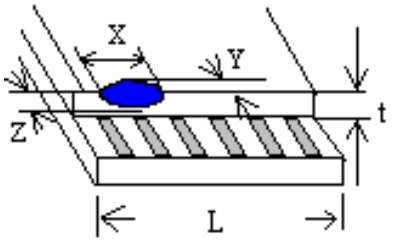
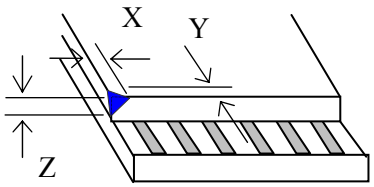
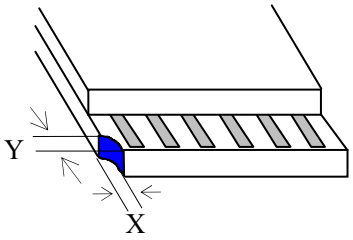
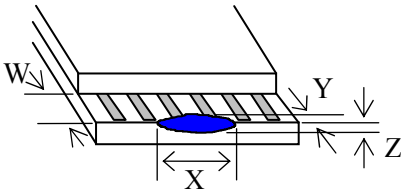
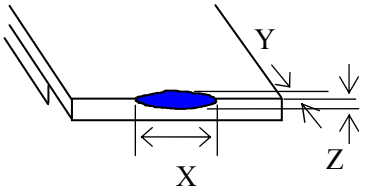
<table>
<tr><th>No.</th><th>Item</th><th>Criterion</th></tr>
<tr><td rowspan="6">1</td><td>Short or open circuit</td><td rowspan="6">Not allow</td></tr>
<tr><td>LC leakage</td></tr>
<tr><td>Flickering</td></tr>
<tr><td>No display</td></tr>
<tr><td>Wrong viewing direction</td></tr>
<tr><td>Wrong Back-light</td></tr>
<tr><td rowspan="2">2</td><td>Contrast defect</td><td rowspan="2">Refer to approval sample</td></tr>
<tr><td>Background color deviation</td></tr>
<tr><td>3</td><td>Point defect,
Black spot, dust
(including Polarizer)

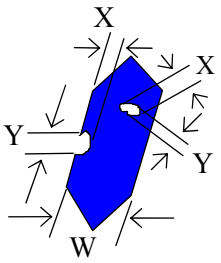
ϕ = (X+Y)/2</td><td> 

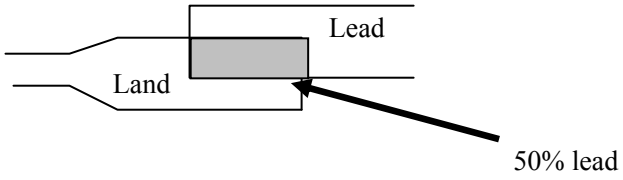
<table>
<tr><th>Point Size</th><th>Acceptable Qty.</th></tr>
<tr><td>ϕ≤0.10</td><td>Disregard</td></tr>
<tr><td>0.10<ϕ≤0.15</td><td>2</td></tr>
<tr><td>0.15<ϕ≤0.25</td><td>1</td></tr>
<tr><td>ϕ>0.25</td><td>0</td></tr>
</table>
Unit：Inch^2</td></tr>
<tr><td>4</td><td>Line defect,

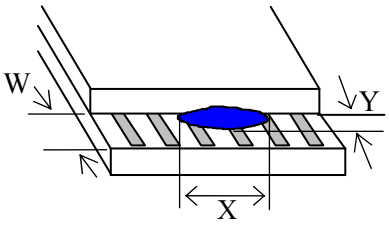
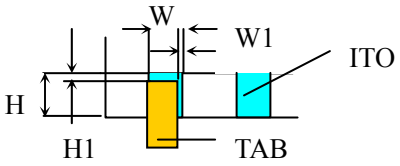
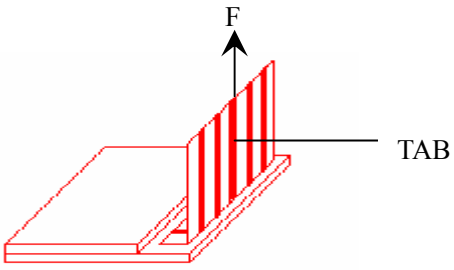
Scratch</td><td> 

<table>
<tr><th colspan="2">Line</th><th>Acceptable Qty.</th></tr>
<tr><th>L</th><th>W</th><th></th></tr>
<tr><td>---</td><td>0.05>W</td><td rowspan="3">Disregard</td></tr>
<tr><td>3.0>L</td><td>0.1>W>0.05</td></tr>
<tr><td>2.0>L</td><td>0.15≥W>0.1</td></tr>
</table>
Unit: mm</td></tr>
<tr><td>5</td><td>Rainbow</td><td>Not more than two color changes across the viewing area.</td></tr>
</table>

No	Item	Criterion
6	Chip Remark: X: Length Y: Width Z: Thickness t: Glass thickness W: Terminal width L: Glass length	 Acceptable criterion X: < L /8; Y: 0.5mm; Z: ≤t/2  Acceptable criterion X: ≤2; Y: 0.5mm; Z: ≤t  Acceptable criterion X: ≤3; Y: ≤2; Z: ≤t shall not reach to ITO  Acceptable criterion X: Disregard; Y: ≤0.2; Z: ≤t  Acceptable criterion X: ≤5; Y: ≤2; Z: ≤t/3

<table>
<tr><th>No.</th><th>Item</th><th>Criterion</th></tr>
<tr><td>7</td><td>Segment
pattern
W = Segment width
ϕ = (X+Y)/2</td><td>(1) Pin hole
ϕ < 0.10mm is acceptable.
 

<table>
<tr><th>Point Size</th><th>Acceptable Qty</th></tr>
<tr><td>ϕ≤1/4W</td><td>Disregard</td></tr>
<tr><td>1/4W< ϕ≤1/2W</td><td>1</td></tr>
<tr><td>ϕ>1/2W</td><td>0</td></tr>
</table>
Unit: mm</td></tr>
<tr><td>8</td><td>Back-light</td><td>(1) The color of backlight should correspond its specification.
(2) Not allow flickering</td></tr>
<tr><td>9</td><td>Soldering</td><td>(1) Not allow heavy dirty and solder ball on PCB.
(The size of dirty refer to point and dust defect)
(2) Over 50% of lead should be soldered on Land.
 
</td></tr>
<tr><td>10</td><td>Wire</td><td>(1) Copper wire should not be rusted
(2) Not allow crack on copper wire connection.
(3) Not allow reversing the position of the flat cable.
(4) Not allow exposed copper wire inside the flat cable.</td></tr>
<tr><td>11*</td><td>PCB</td><td>(1) Not allow screw rust or damage.
(2) Not allow missing or wrong putting of component.</td></tr>
</table>

No	Item	Criterion
12	Protruded W: Terminal Width	 Acceptable criteria: Y ≤ 0.4
13	TAB	1. Position  W1≤1/3W H1≤1/3H 2 TAB bonding strength test  P (=F/TAB bonding width) ≥650gf/cm ,(speed rate: 1mm/min) 5pcs per SOA (shipment)
14	Total no. of acceptable Defect	A. Zone Maximum 2 minor non-conformities per one unit. Defect distance: each point to be separated over 10mm B. Zone It is acceptable when it is no trouble for quality and assembly in customer's end product.

Electrical and optical inspection

Electrical and Optical Parameters of LCM

ITEM	SYMBOL	STN Dot Matrix Character Type			UNIT
		MIN.	TYP.	MAX.	
LCD Operating Voltage	V_{LCD}	-	5.0	-	V
Contrast	Cr	10:1			-
Response Time (25℃)	t_r		150	250	ms
	t_d		150	250	
Viewing Angle (Cr=3)	θ	45	-	60	deg
	Φ	-40	-	40	
Operating Temp.	T_{OP}	-20~+70			°C
Storage Temp.	T_{ST}	-25~+80			
Minimum Life Time	τ	≥50000			h

Reliability of LCM

Reliability test

Items of reliability test are as the followings with no abnormalities and function failures found after the test: (Number of specimen: 16)

Item	Condition	Time (hrs)	Assessment
High temp. Storage	80°C	96	No abnormalities in functions and appearance
High temp. Operating	70°C	96	
Low temp. Storage	-30°C	96	
Low temp. Operating	-20°C	96	
Humidity	40°C/ 90%RH	96	
Temperature shock	-20°C ← 25°C →70°C (30 min ← 5 min → 30min)	12 cycles	

Recovery time should be 12 hours minimum.

Vibration test

10~55Hz and amplitude 1.5mm at X, Y and Z direction for 2 hours each

Drop test

Drop shock from height of 1m, 10pcs in packing

General Precautions:

1. LCD panel is made of glass. Avoid excessive mechanical shock or applying strong pressure onto the surface of display area.
2. The polarizer used on the display surface is easily scratched and damaged. Extreme care should be taken when handling. To clean dust or dirt off the display surface, wipe gently with cotton, or other soft material soaked with isoproply alcohol or ethyl alcohol, do not use water, ketone or aromatics and never scrub LCD hard.
3. Do not tamper in any way with the tabs on the metal frame.
4. Do not make any modification on the PCB without consulting XIAMEM OCULAR
5. When mounting a LCM, make sure that the PCB is not under any stress such as bending or twisting. Elastomer contacts are very delicate and missing pixels could result from slight dislocation of any of the elements.
6. Avoid pressing on the metal bezel, otherwise the elastomer connector could be deformed and lose contact, resulting in missing pixels and also cause rainbow on the display.
7. Be careful not to touch or swallow liquid crystal that might leak from a damaged cell. Any liquid crystal sprays on skin or clothes, please wash it off immediately with water.

Static Electricity Precautions:

1. CMOS-LSI is used for the module circuit; therefore operators should be grounded whenever he/she comes into contact with the module.
2. Do not touch any of the conductive parts such as the LSI pads; the copper leads on the PCB and the interface terminals with any parts of the human body.
3. Do not touch the connection terminals of the display with bare hand; it will cause disconnection or defective insulation of terminals.
4. The modules should be kept in anti-static bags or other containers resistant to static for storage.
5. Only properly grounded soldering irons should be used.
6. If an electric screwdriver is used, it should be grounded and shielded to prevent sparks.
7. The normal static prevention measures should be observed for work clothes and working benches.
8. Since dry air is inductive to static, a relative humidity of 50-60% is recommended.

Soldering Precautions:

1. Soldering should be performed only on the I/O terminals.
2. Use soldering irons with proper grounding and no leakage.

3. Soldering temperature: 280°C±10°C
4. Soldering time: 3 to 4 second.
5. Use eutectic solder with resin flux filling.
6. If flux is used, the LCD surface should be protected to avoid spattering flux.
7. Flux residue should be removed.

Operation Precautions:

1. The viewing angle can be adjusted by varying the LCD driving voltage Vo.
2. Since applied DC voltage causes electro-chemical reactions, which deteriorate the display, the applied pulse waveform should be a symmetric waveform such that no DC component remains. Be sure to use the specified operating voltage.
3. Driving voltage should be kept within specified range; excess voltage will shorten display life.
4. Response time increases with decrease in temperature.
5. Display color may be affected at temperatures above its operational range.
6. Keep the temperature within the specified range usage and storage. Excessive temperature and humidity could cause polarization degradation, polarizer peel-off or generate bubbles.
7. For long-term storage over 40°C is required, the relative humidity should be kept below 60%, and avoid direct sunlight.