RAM Mapping 60×16 LCD Controller Driver

HT16H25

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Features

- Logic Operating Voltage: 2.4V~5.5V
- Analog Operating Voltage: 2.4V~5.5V
- LCD Operating Voltage (V_{LCD}): 2.5V~12V
- LCD display data RAM: 120×8 bits=960 bits
- LCD display: Max. 60 segments and 16 commons
- Bias: 1/1, 1/2, 1/3, 1/4, 1/5; Duty: static, 1/2~1/16
- Internal LCD bias generated from charge pump or resistor divider
- Internal RC oscillator
- Four general purpose output (GPO) ports
- GPO ports support binary output or PWM output with 64-level PWM control
- Integrated Charge Pump
- Contrast Adjustment Function
- Support I^2C-bus or SPI 3-wire serial interface
- Selectable LCD frame frequencies
- Four selectable blinking frequencies
- Selectable A type or B type LCD driving waveform
- Package type: 80/100-pin LQFP

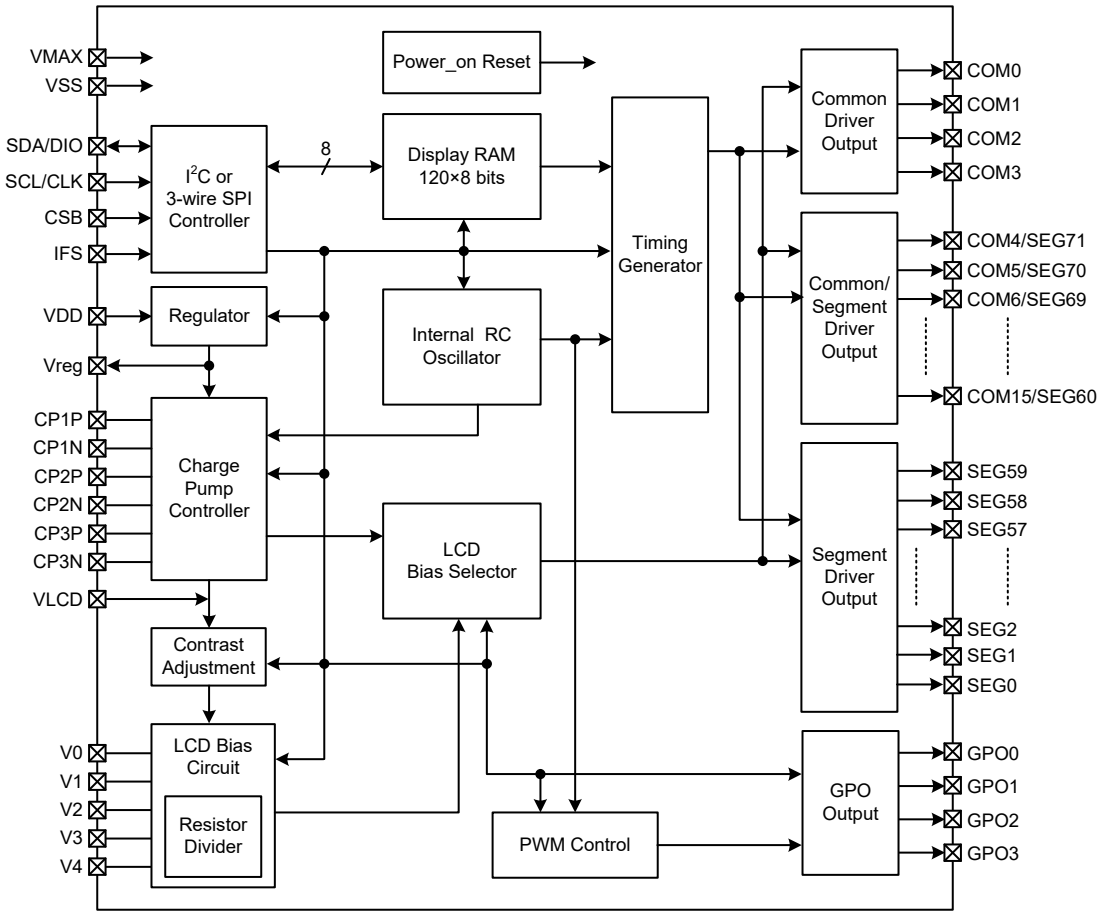
Applications

- Car display
- Leisure products
- Audio Combo display
- Video Player display
- Household appliance
- Consumer electronics

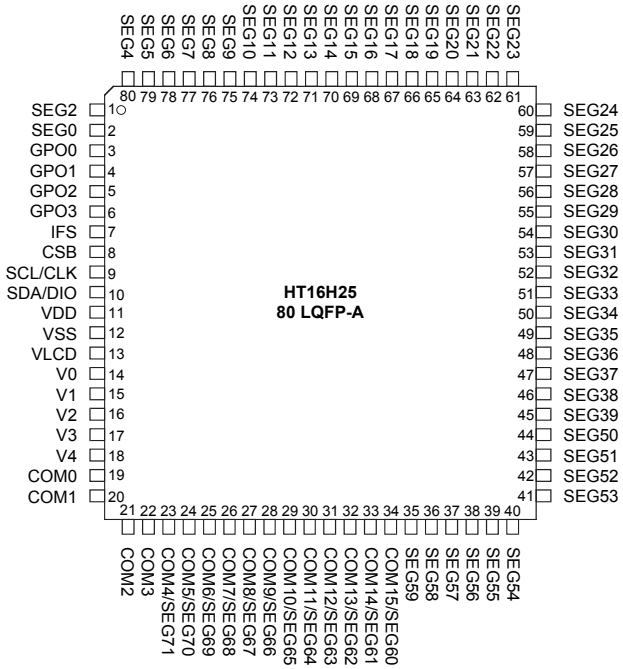
General Description

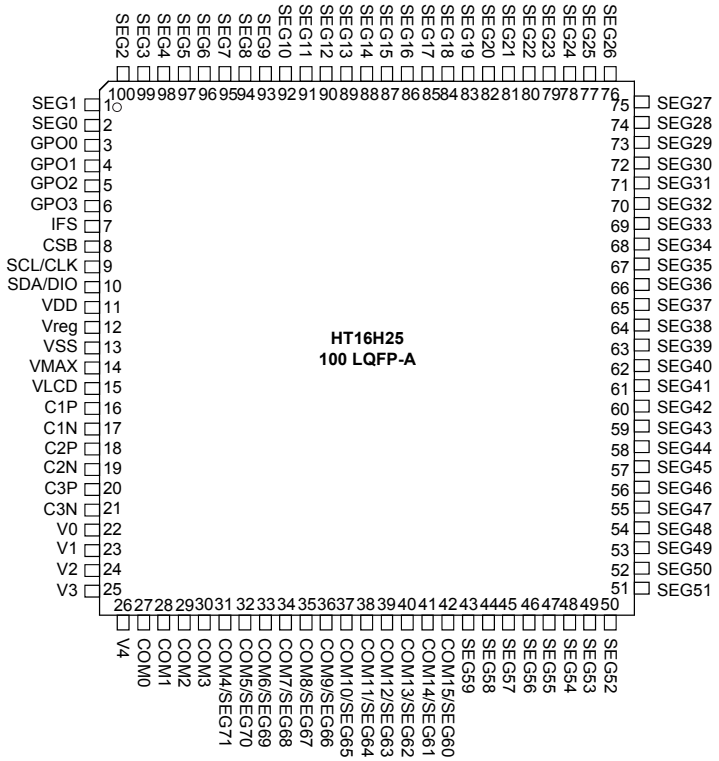
The HT16H25 is a memory mapping and multi-function LCD controller driver which can be switched to multi-duty. It can display up to 960 patterns for 1/16 duty. It supports up to 4 port GPO outputs to control other devices. The GPO outputs also can be set as PWM outputs with 64-level PWM control to drive LED backlight. The HT16H25 is compatible with most microprocessors/ microcontrollers and communicates via a 2-wire I^2C-bus or a 3-wire SPI serial interface.

Block Diagram



Pin Assignment



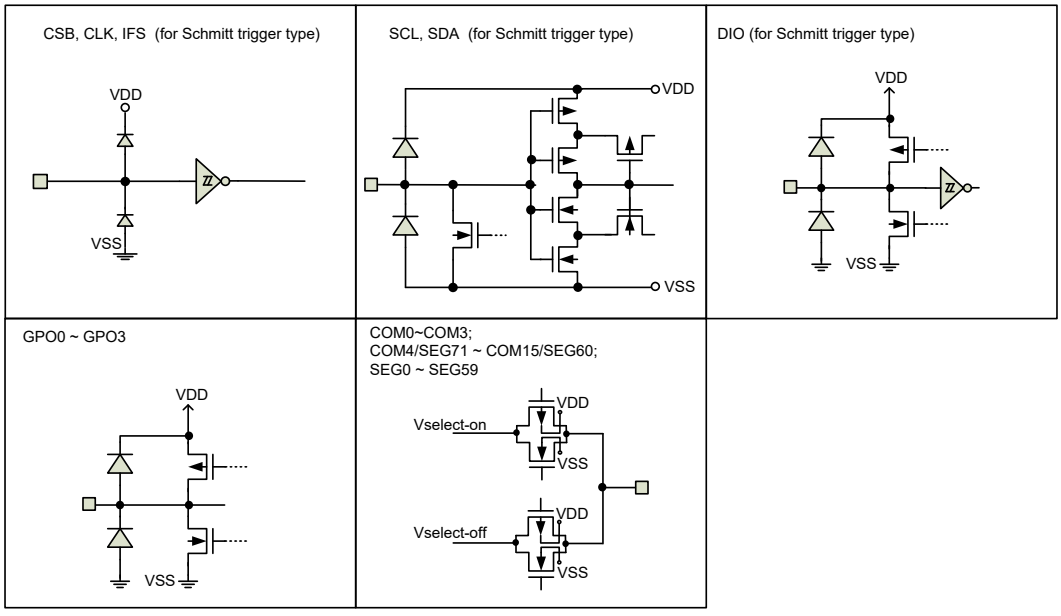


Note: For HT16H25 80-pin LQFP, the charge pump function is invalid and is forbidden to be used. For normal operation, the LCD bias circuit select command has to be set as 00010011b, which means that V_{LCD} is supplied from the external power and the LCD bias is generated by a resistor divider. The power condition: $V_{LCD} \geq V_{DD}$.

Pin Description

Pin Name	Type	Description
VDD	—	Positive power supply
VSS	—	Negative power supply, ground
VLCD	—	LCD power supply pin
VMAX	I	LCD driver circuit maximum reference voltage pin Connected to the greatest voltage of V_{DD}, V_{LCD} and V0
Vreg	O	Internal regulator output. Bypass to VSS with 1μF or 4.7μF (1~10μF)
CSB	I	SPI Chip Select pin This pin is active low and only available for SPI 3-wire interface. When the I^2C interface is used, this pin is not used and must be connected to VDD.
SCL/CLK	I	Serial clock input pin. ● Serial Clock (SCL) Input for I^2C interface ● Serial Clock (CLK) Input for SPI 3-wire serial interface
SDA/DIO	I/O	Serial data input/output pin. Data is input to or comes out from the shift register at the clock rising edge. ● I^2C interface Serial Data (SDA) Input / Output – NMOS open-drain output ● SPI 3-wire interface Serial Data (DIO) Input / Output – CMOS output
IFS	I	Communication interface select pin ● IFS=VDD, the device communicates with MCU via 2-wire I^2C interface. ● IFS=VSS, the device communicates with MCU via 3-wire SPI interface.
C1P, C1N	—	Flying capacitor pins. A capacitor should be connected between C1P and C1N
C2P, C2N	—	Flying capacitor pins. A capacitor should be connected between C2P and C2N
C3P, C3N	—	Flying capacitor pins. A capacitor should be connected between C3P and C3N
V0~V4	—	LCD bias voltage pin
GPO0~GPO3	O	General purpose outputs
COM0~COM3	O	LCD Common outputs
COM4/SEG71~ COM15/SEG60	O	LCD common / segment multiplexed driver outputs
SEG0~SEG59	O	LCD Segment outputs

Approximate Internal Connections



Absolute Maximum Ratings

Logic Supply Voltage ..... V_{SS}-0.3V to V_{SS}+6.5V

Driver Supply Voltage ..... Vss-0.3V to Vss+13.2V

Input Voltage ..... V_{SS}-0.3V to V_{DD}+0.3V

Storage Temperature ..... -60°C to 150°C

Operating Temperature ..... -40°C to 85°C

Note: These are stress ratings only. Stresses exceeding the range specified under "Absolute Maximum Ratings" may cause substantial damage to the device. Functional operation of this device at other conditions beyond those listed in the specification is not implied and prolonged exposure to extreme conditions may affect device reliability.

D.C. Characteristics

V_{SS}=0V, V_{DD}=2.4V~5.5V, Ta=-40°C~85°C

Symbol	Parameter	Test condition		Min.	Typ.	Max.	Unit
		V_{DD}	Condition				
V_{DD}	Logic Operating Voltage	—	—	2.4	—	5.5	V
V_{LCD}	LCD Operating Voltage	—	—	2.5	—	12	V
V_{reg}	Regulator Output Voltage	5V	Regulator output=2.4V	2.28	2.4	2.52	V
I_{STB1}	V_{DD} Standby Current	3.3V	No load, All analog circuits off All registers are set to default value	—	—	1	μA
		5V		—	—	2	μA
I_{STB2}	V_{LCD} Standby Current	3.3V	No load, All analog circuits off All registers are set to default value	—	—	1	μA
		5V		—	—	2	μA
I_{DD}	V_{DD} Operating Current	3.3V	No load, LCD Display off, Internal oscillator on, PWM disable Other settings are set to default value	—	5	10	μA
		5V		—	10	20	μA
I_{DD1}	V_{DD} Operating Current	3.3V	No load, LCD Display off, Internal oscillator on, PWM enable Other settings are set to default value	—	15	30	μA
		5V		—	25	50	μA
I_{DD2}	V_{DD} Operating Current	3.3V	No load, LCD Display on, Internal oscillator on, PWM disable Regulator Voltage=2.4V Charge pump ratio=×5 LCD bias circuit=charge pump Other settings are set to default value	—	260	520	μA
		5V		—	240	480	μA
I_{DD3}	V_{DD} Operating Current	3.3V	No load, LCD Display on, Internal oscillator on, PWM enable Regulator Voltage=2.4V Charge pump ratio=×5 LCD bias circuit=charge pump Other settings are set to default value	—	280	560	μA
		5V		—	260	520	μA
I_{VLCD}	V_{LCD} Operating Current	5.5V	No load, LCD Display on, V_{LCD}=12V, Bias circuit=resistor divider Other settings are set to default value	—	180	360	μA
V_{IH}	Input High Voltage	—	CSB, CLK, DIO	0.7V_{DD}	—	V_{DD}	V
V_{IL}	Input Low Voltage	—	CSB, CLK, DIO	0	—	0.3V_{DD}	V
I_{IL}	Input Leakage Current	—	V_{IN}=V_{SS} or V_{DD}	-1	—	1	μA
I_{OH}	High Level Output Current	3.3V	V_{OH}=0.9V_{DD} for DIO, GPO	-6	—	—	mA
		5V		-12	—	—	mA
I_{OL}	Low Level Output Current	3.3V	V_{OL}=0.4V for SDA, DIO, GPO	6	—	—	mA
		5V		3	—	—	mA

Symbol	Parameter	Test condition		Min.	Typ.	Max.	Unit
		V_{DD}	Condition				
I_{OH1}	LCD Common Source Current	—	V_{LCD}=12V, V_{OH}=10.8V	-8.4	-14	—	mA
			V_{LCD}=5V, V_{OH}=4.5V	-2.1	-3.5	—	mA
I_{OL1}	LCD Common Sink Current	—	V_{LCD}=12V, V_{OL}=1.2V	16.8	28	—	mA
			V_{LCD}=5V, V_{OL}=0.5V	4.2	7	—	mA
I_{OH2}	LCD Segment Source Current	—	V_{LCD}=12V, V_{OH}=11.8V	-4.8	-8	—	mA
			V_{LCD}=5V, V_{OH}=4.5V	-1.2	-2	—	mA
I_{OL2}	LCD Segment Sink Current	—	V_{LCD}=12V, V_{OL}=1.2V	9.6	16	—	mA
			V_{LCD}=5V, V_{OL}=0.5V	2.4	4	—	mA

A.C. Characteristics

V_{SS}=0V, V_{DD}=2.4V~5.5V, Ta=-40°C~85°C

Symbol	Parameter	Test Condition		Min.	Typ.	Max.	Unit
		V_{DD}	Condition				
f_{OSC1}	Oscillator Frequency	3.3V	—	221.84	245.76	270.33	kHz
f_{OSC2}	Oscillator Frequency	3.3V	—	55.26	61.4	67.54	kHz
f_{LCD}	LCD Frame Frequency	3.3V	F[3:0]=1010, duty=1/16	180	200	220	Hz
V_{POR}	V_{DD} Start Voltage to ensure Power-on Reset	—	—	0.05	—	0.1	V
RR_{POR}	V_{DD} Rise Rate to ensure Power-on Reset	—	—	0.05	—	—	V/ms
t_{POR}	Minimum Time for V_{DD} to remain at V_{POR} to ensure Power-on Reset	—	—	10	—	—	ms

A.C. Characteristics – I²C Interface

V_{SS}=0V, V_{DD}=2.4V~5.5V, Ta=-40°C~85°C

Symbol	Parameter	Condition	V_{DD}=2.4V~5.5V		V_{DD}=3.0V~5.5V		Unit
			Min.	Max.	Min.	Max.	
f_{SCL}	Clock Frequency	—	—	100	—	400	kHz
t_{BUF}	Bus Free Time	Time in which the bus must be free before a new transmission can start	4.7	—	1.3	—	μs
$t_{HD: STA}$	Start Condition Hold Time	After this period, the first clock pulse is generated	4	—	0.6	—	μs
t_{LOW}	SCL Low Time	—	4.7	—	1.3	—	μs
t_{HIGH}	SCL High Time	—	4	—	0.6	—	μs
$t_{SU: STA}$	Start Condition Setup Time	Only relevant for repeated START condition	4.7	—	0.6	—	μs
$t_{HD: DAT}$	Data Hold Time	—	0	—	0	—	ns
$t_{SU: DAT}$	Data Setup Time	—	250	—	100	—	ns
t_R	SDA and SCL Rise Time	Note	—	1	—	0.3	μs
t_F	SDA and SCL Fall Time	Note	—	0.3	—	0.3	μs
$t_{SU: STO}$	Stop Condition Set-up Time	—	4	—	0.6	—	μs
t_{AA}	Output Valid from Clock	—	—	3.5	—	0.9	μs
t_{SP}	Input Filter Time Constant (SDA and SCL Pins)	Noise suppression time	—	100	—	50	ns

Note: These parameters are periodically sampled but not 100% tested.

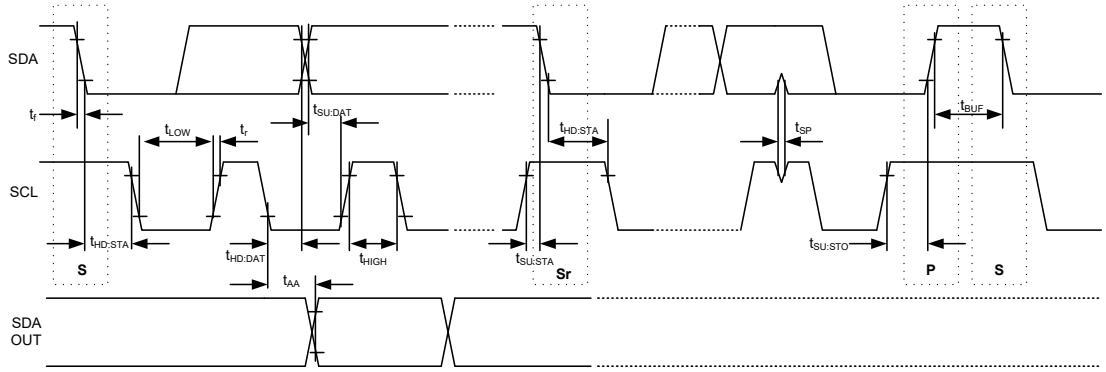
A.C. Characteristics – SPI 3-wire Serial Interface

V_{SS}=0V, V_{DD}=2.4V~5.5V, Ta=-40°C~85°C

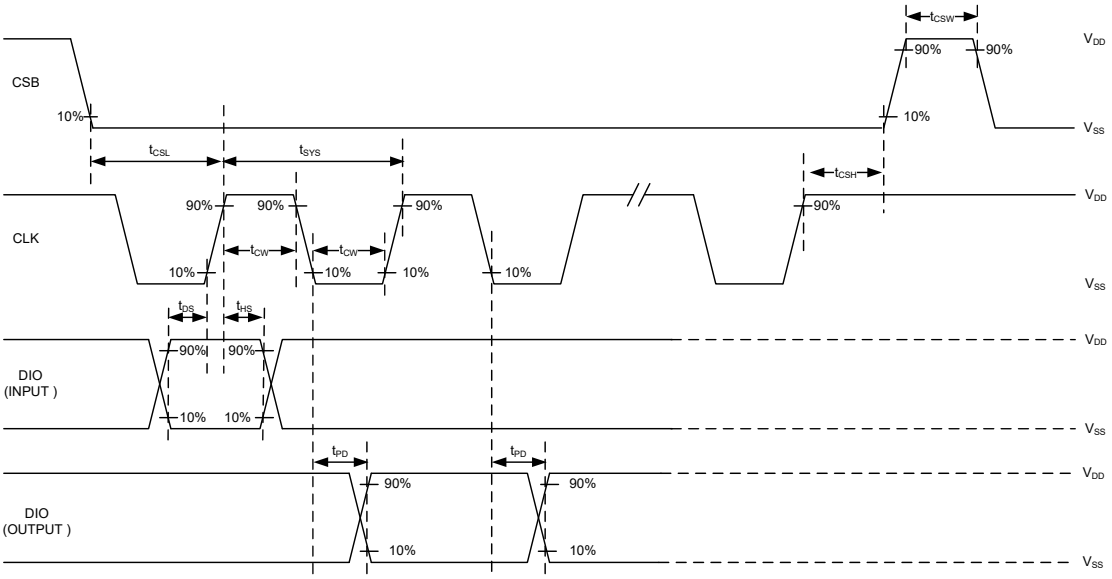
Symbol	Parameter	Test Condition			Min.	Typ.	Max.	Unit
		V_{DD}	Condition					
t_{SYS}	Clock cycle time	—	For write data		250	—	—	ns
			For read data		1000	—	—	ns
t_{CW}	Clock Pulse Width	—	For write data		50	—	—	ns
			For read data		400	—	—	ns
t_{DS}	Data Setup Time	—	For write data		50	—	—	ns
t_{DH}	Data Hold Time	—	For write data		50	—	—	ns
t_{CSW}	"H" CSB Pulse Width	—	—		50	—	—	ns
t_{CSL}	CSB Setup Time (CSB↓ – CLK↑)	—	For write data		50	—	—	ns
			For read data		400	—	—	ns
t_{CSH}	CS Hold Time (CLK↑ – CSB↑)	—	—		2	—	—	μs
t_{PD}	DATA Output Delay Time (CLK – DIO)	—	C_O=15pF	t_{PD}=10% to 90%	—	—	350	ns
				t_{PD}=10% to 10%				

Timing Diagrams

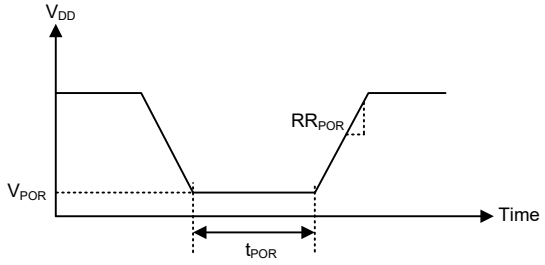
I²C Bus Timing



SPI 3-wire Bus Timing



Reset Timing



Note: 1. If the reset timing conditions are not satisfied during the power ON/OFF sequence, the internal Power on Reset (POR) circuit will not operate normally.

2. If it is difficult to meet power on reset timing conditions, execute software reset command after Power on.

Functional Description

Power-on Reset

When power is turned on, the device is initialised by an internal power-on reset circuit. The internal circuit status after initialisation is as follows:

- All registers are set to their default value but the contests of the RAM are not affected.
- The drive mode with 1/16 duty and 1/5 bias is selected.
- The System Oscillator is off
- The LCD Display is in an off state.
- All common outputs are set to V_{SS}.
- All segment outputs are set to V_{SS}.
- All GPO outputs are set to V_{SS}.
- The Internal regulator is disabled.
- The Charge pump is off.
- The LCD bias circuit is off.
- The GPO pins are set as binary mode.
- The Frame Frequency is set to 200Hz.
- The Blinking Frequency is set to off.

Data transfers on the I^2C-bus or SPI 3-wire serial bus should be avoided for 1ms following a power-on to allow the reset initialisation operation to complete.

System Oscillator

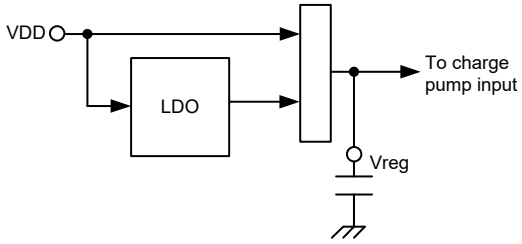
The timing for the internal logic, the LCD driver signals and the PWM signals are generated by an internal oscillator. The System Clock frequency (f_{SYS}) determines the LCD frame frequency and the PWM frame frequency.

Internal Regulator

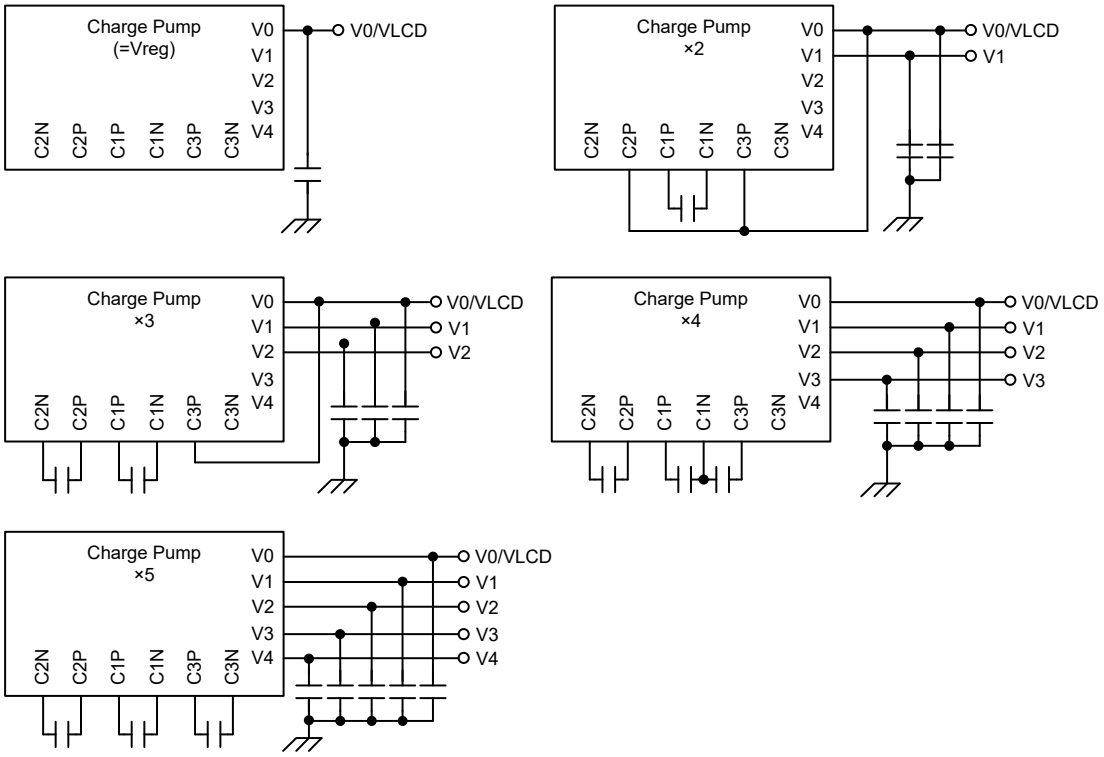
The internal regulator is used for the charge pump input. The regulator output can be set from 1.0V to 4.1V. The regulator output ready time is about 200ms. The Vreg pin is the regulator output and bypasses with a capacitor to VSS. Note that $V_{reg} \leq V_{DD}$-0.2V.

Charge Pump

The charge pump is used to generate the V_{LCD}, which is the LCD driving voltage. The input voltage can be supplied from the V_{DD} or the internal regulator using commands. The circuit diagram is shown below.



The charge pump ratio can be set to ×2, ×3, ×4 or ×5. The charge pump configuration is shown below. Due to process limitation, the V0 or V_{LCD} cannot be greater than 12V, which is forbid to use.



The relationship between the charge pump input voltage, the charge pump ratio and the output voltage is shown in the following table. Note that it is forbidden to use when the charge pump output voltage is greater than 12V.

Charge Pump Input Voltage		Charge Pump Output Voltage (V)				
Regulator	1.0	1.0	2.0	3.0	4.0	5.0
	1.1	1.1	2.2	3.3	4.4	5.5
	1.2	1.2	2.4	3.6	4.8	6.0
	1.3	1.3	2.6	3.9	5.2	6.5
	1.4	1.4	2.8	4.2	5.6	7.0
	1.5	1.5	3.0	4.5	6.0	7.5
	1.6	1.6	3.2	4.8	6.4	8.0
	1.7	1.7	3.4	5.1	6.8	8.5
	1.8	1.8	3.6	5.4	7.2	9.0
	1.9	1.9	3.8	5.7	7.6	9.5
	2.0	2.0	4.0	6.0	8.0	10.0
	2.1	2.1	4.2	6.3	8.4	10.5
	2.2	2.2	4.4	6.6	8.8	11.0
	2.3	2.3	4.6	6.9	9.2	11.5
	2.4	2.4	4.8	7.2	9.6	12.0
	2.5	2.5	5.0	7.5	10.0	12.5
	2.6	2.6	5.2	7.8	10.4	13.0
×2, 1/2 bias →		V1	V0			
×3, 1/3 bias →		V2	V1	V0		
×4, 1/4 bias →		V3	V2	V1	V0	
×5, 1/5 bias →		V4	V3	V2	V1	V0

Charge Pump Input Voltage		Charge Pump Output Voltage (V)				
Regulator	2.7	2.7	5.4	8.1	10.8	13.5
	2.8	2.8	5.6	8.4	11.2	14.0
	2.9	2.9	5.8	8.7	11.6	14.5
	3.0	3.0	6.0	9.0	12.0	15.0
	3.1	3.1	6.2	9.3	12.4	15.5
	3.2	3.2	6.4	9.6	12.8	16.0
	3.3	3.3	6.6	9.9	13.2	16.5
	3.4	3.4	6.8	10.2	13.6	17.0
	3.5	3.5	7.0	10.5	14.0	17.5
	3.6	3.6	7.2	10.8	14.4	18.0
	3.7	3.7	7.4	11.1	14.8	18.5
	3.8	3.8	7.6	11.4	15.2	19.0
	3.9	3.9	7.8	11.7	15.6	19.5
	4.0	4.0	8.0	12.0	16.0	20.0
	4.1	4.1	8.2	12.3	16.4	20.5
V_{DD}	3.3	3.3	6.6	9.9	13.2	16.5
	5	5.0	10.0	15.0	20.0	25.0
×2, 1/2 bias →		V1	V0			
×3, 1/3 bias →		V2	V1	V0		
×4, 1/4 bias →		V3	V2	V1	V0	
×5, 1/5 bias →		V4	V3	V2	V1	V0

Contrast Adjustment

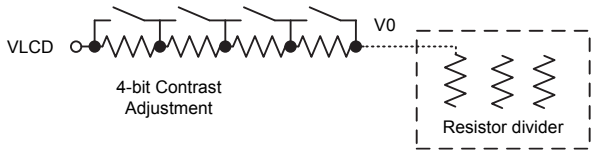
The contrast adjustment is used to adjust the V0. The contrast adjustment specification is shown in the following table for each LCD bias circuit.

Contrast Adjustment	LCD Bias Circuit
No support	Charge Pump
4-bit adjustable	Resistor Divider

The contrast adjustment formula for the resistor divider is shown below.

Resistor	V0 Formula
4K	$V0=V_{LCD}\times\frac{4B}{4B+CA[3:0]\times2}$
8K	$V0=V_{LCD}\times\frac{8B}{8B+CA[3:0]\times2}$
16K	$V0=V_{LCD}\times\frac{16B}{16B+CA[3:0]\times2}$

where B=1/bias, ex: bias=1/5, B=5



LCD Bias Generator

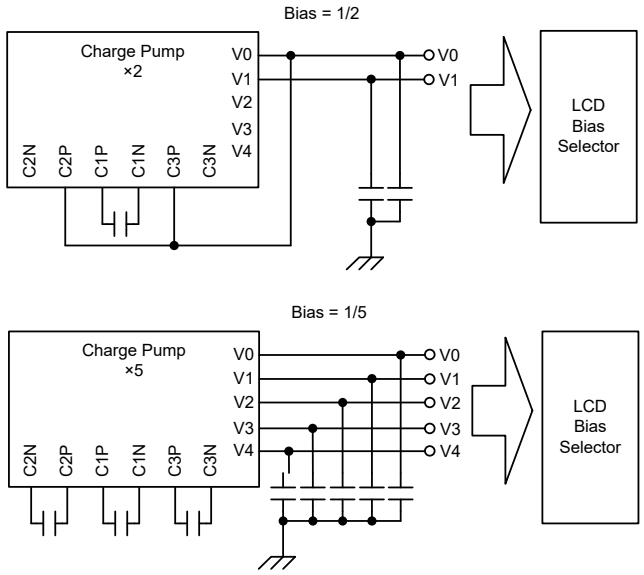
The LCD bias can be generated by the charge pump or the resistor divider using commands.

When the LCD bias generator is set to the charge pump, the LCD bias is generated by the pumping voltage. The charge pump ratio selection is depending on the bias setting, the relationship between LCD bias and charge pump ratio is shown in the following table.

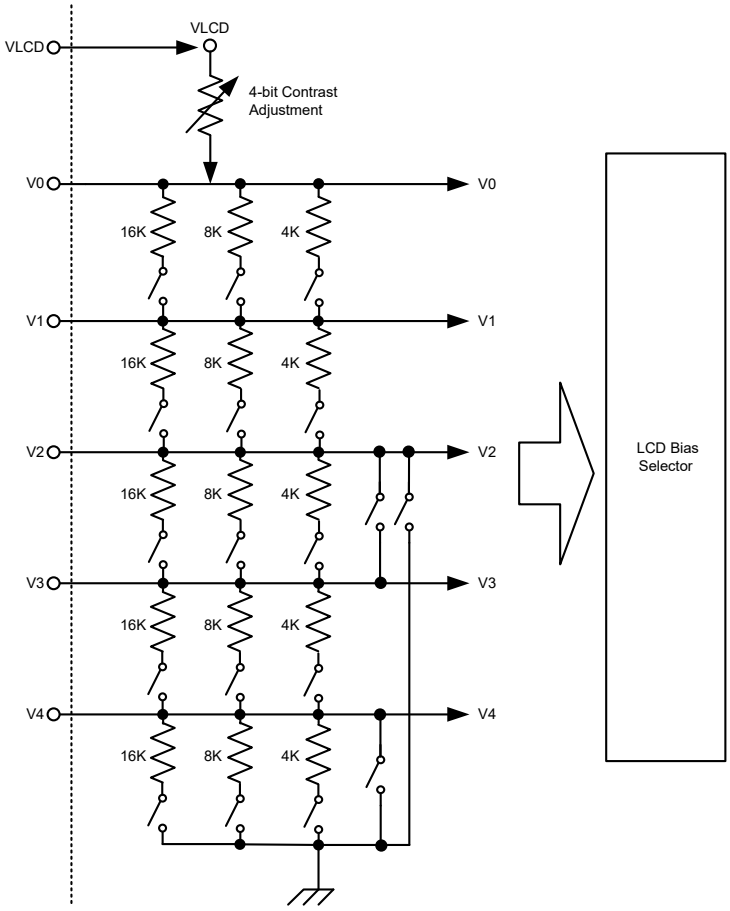
Refer to the “Charge Pump” section to obtain the charge pump configuration for each charge pump ratio. All capacitors connected to the charge pump use 0.1μF. The charge pump output ready time is about 20ms.

LCD Bias	Charge Pump Ratio Setting
Static	Charge Pump Input Voltage
1/2	×2
1/3	×3
1/4	×4
1/5	×5

The circuit diagram for LCD 1/2 bias and 1/5 bias are shown below.



When the LCD bias is generated by the resistor divider, there are 3 kinds of resistor values, 4K, 8K and 16K. The V_{LCD} is only supplied from the external VLCD pin.



Common Driver Outputs

The LCD driver section includes common outputs which should be connected directly to the LCD panel. The common output signals are generated in accordance with the selected LCD drive mode. The unused common outputs should be left open-circuit.

Common/Segment Driver Outputs

The common/segment driver can be set as a common or segment driver with LCD configuration. The unused outputs should be left open-circuit.

Segment Driver Outputs

The LCD driver section includes segment outputs which should be connected directly to the LCD panel. The segment output signals are generated in accordance with the multiplexed common signals and with the data resident in the display latch. The unused segment outputs should be left open-circuit.

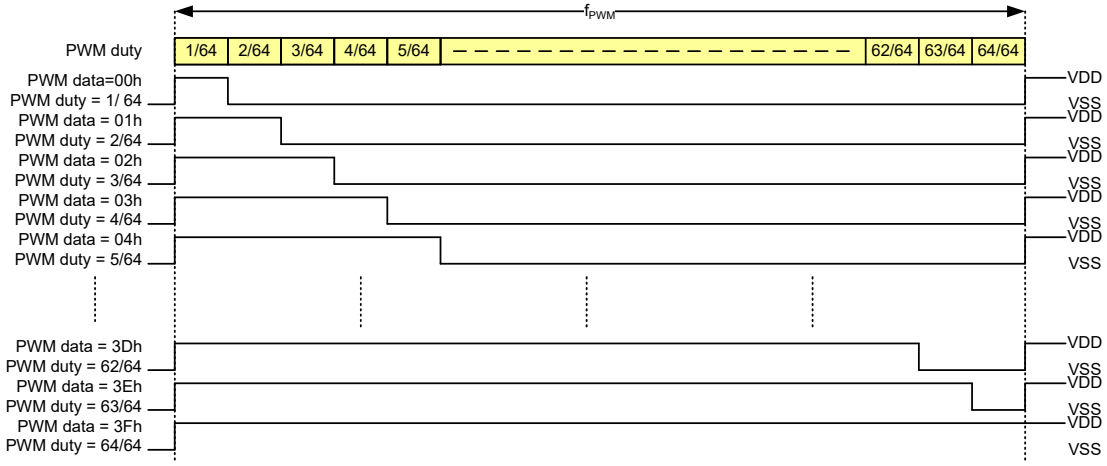
GPO Driver Outputs

The GPO driver is used to connect other devices and output control signals. It also can be set as PWM outputs. There are 64 steps output in PWM outputs. The PWM outputs can be used to control LEDs.

PWM Control

The device supports 64-level PWM control function. The PWM outputs can be set as 1/64~64/64 duty output in each PWM frame frequency. The PWM signal is synchronous with the internal clock. The PWM outputs with different PWM duty settings are shown below.

The PWM frame frequency depends on the LCD frame frequency. Refer to "Frame Frequency Setting Command" for more information.



Display Memory – RAM Structure

The display RAM is a static 60×8×2 bits capacity RAM in which is stored the LCD data. A logic "1" in the RAM bit-map indicates an "on" state of the corresponding LCD segment. Similarly a logic 0 indicates an 'off' state.

There is a one-on-one correspondence between the display memory addresses and the segment outputs, and between the individual bits of a RAM word and the column outputs. The following shows the mapping from the RAM to the LCD pattern.

The page memory function is supported when the duty is less than or equal to 1/8, user can write display data to page 0 RAM and page 1 RAM, then choose which page memory to display using commands.

The following shows the maximum memory address and the valid commons for each duty.

Duty	Max. Memory Address
1/16	77h
1/15	79h
1/14	7Bh
1/13	7Dh
1/12	7Fh
1/11	81h
1/10	83h
1/9	85h
1/8	43h
1/7	44h
1/6	45h
1/5	46h
1/4, 1/3, 1/2, static	47h

Duty	Vaild Commons
1/16	C0M0~COM15
1/15	COM0~COM14
1/14	COM0~COM13
1/13	COM0~COM12
1/12	COM0~COM11
1/11	COM0~COM10
1/10	COM0~COM9
1/9	COM0~COM8
1/8	COM0~COM7
1/7	COM0~COM6
1/6	COM0~COM5
1/5	COM0~COM4
1/4	COM0~COM3
1/3	COM0~COM2
1/2	COM0, COM1
static	COM0

The following shows the memory map for duty=1/16~1/9.

		D7	D6	D5	D4	D3	D2	D1	D0	Data	D7	D6	D5	D4	D3	D2	D1	D0	Data
		COM15	COM14	COM13	COM12	COM11	COM10	COM9	COM8	Address	COM7	COM6	COM5	COM4	COM3	COM2	COM1	COM0	Address
	SEG0									01h									00h
	SEG1									03h									02h
	SEG2									05h									04h
	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:
	SEG56									71h									70h
	SEG57									73h									72h
duty	SEG58									75h									74h
1/16	SEG59									77h									76h
1/15	SEG60									79h									78h
1/14	SEG61									7Bh									7Ah
1/13	SEG62									7Dh									7Ch
1/12	SEG63									7Fh									7Eh
1/11	SEG64									81h									80h
1/10	SEG65									83h									82h
1/9	SEG66									85h									84h

The following shows the memory map for duty=1/8~1/5, 1/4~static.

	Page 0, PM="0"										Page 1, PM="1"									
		D7	D6	D5	D4	D3	D2	D1	D0	Data		D7	D6	D5	D4	D3	D2	D1	D0	Data
		COM7	COM6	COM5	COM4	COM3	COM2	COM1	COM0	Address		COM7	COM6	COM5	COM4	COM3	COM2	COM1	COM0	Address
	SEG0									00h	SEG0									00h
	SEG1									01h	SEG1									01h
	SEG2									02h	SEG2									02h
	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:
	SEG64									40h	SEG64									40h
	SEG65									41h	SEG65									41h
duty	SEG66									42h	SEG66									42h
8	SEG67									43h	SEG67									43h
7	SEG68									44h	SEG68									44h
6	SEG69									45h	SEG69									45h
5	SEG70									46h	SEG70									46h
1,2,3,4	SEG71									47h	SEG71									47h

The following shows a data transfer format for I²C or SPI 3-wire serial interface.

MSB LSB

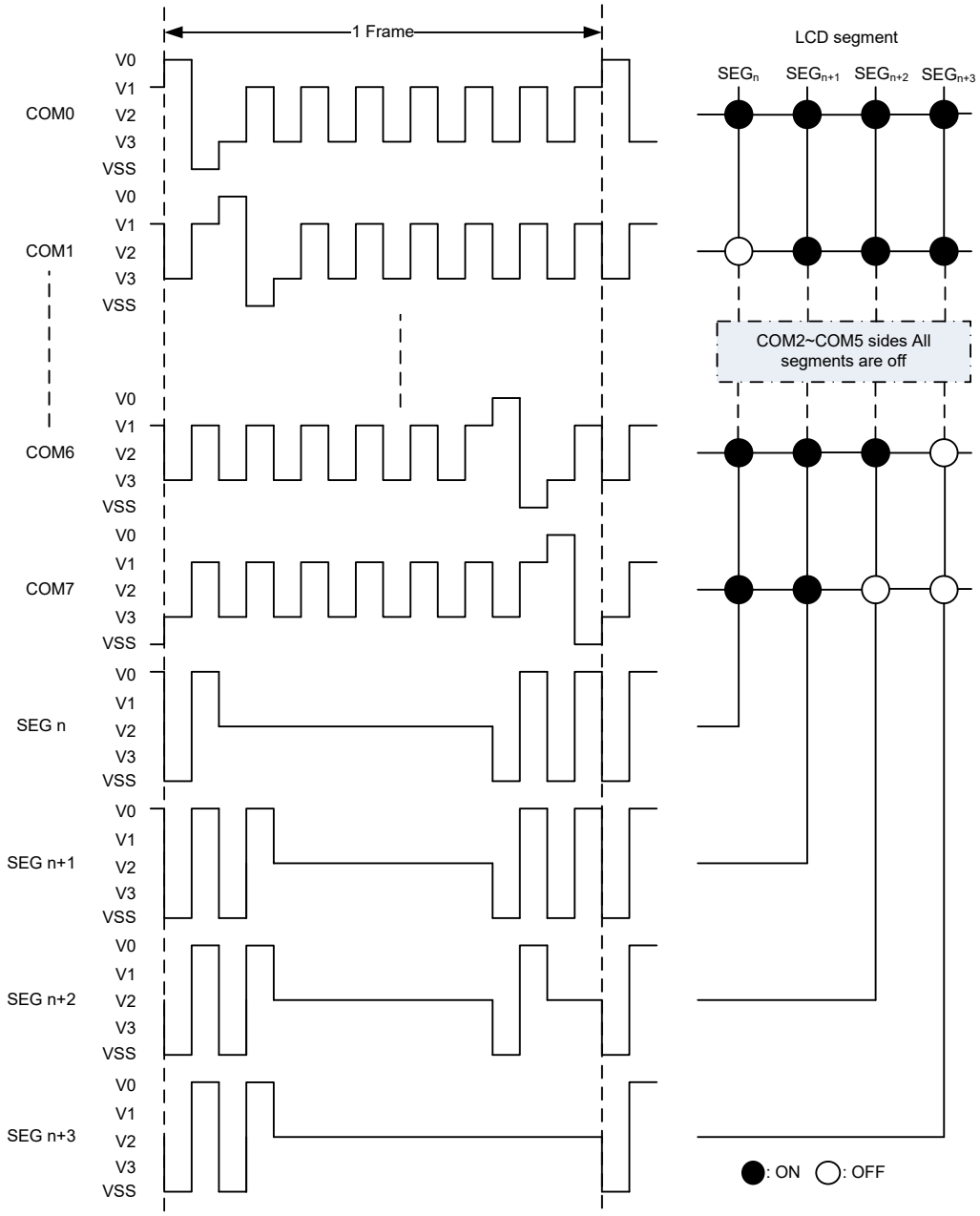
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
D7	D6	D5	D4	D3	D2	D1	D0

LCD Drive Mode Waveforms

The following shows a part of LCD drive waveforms.

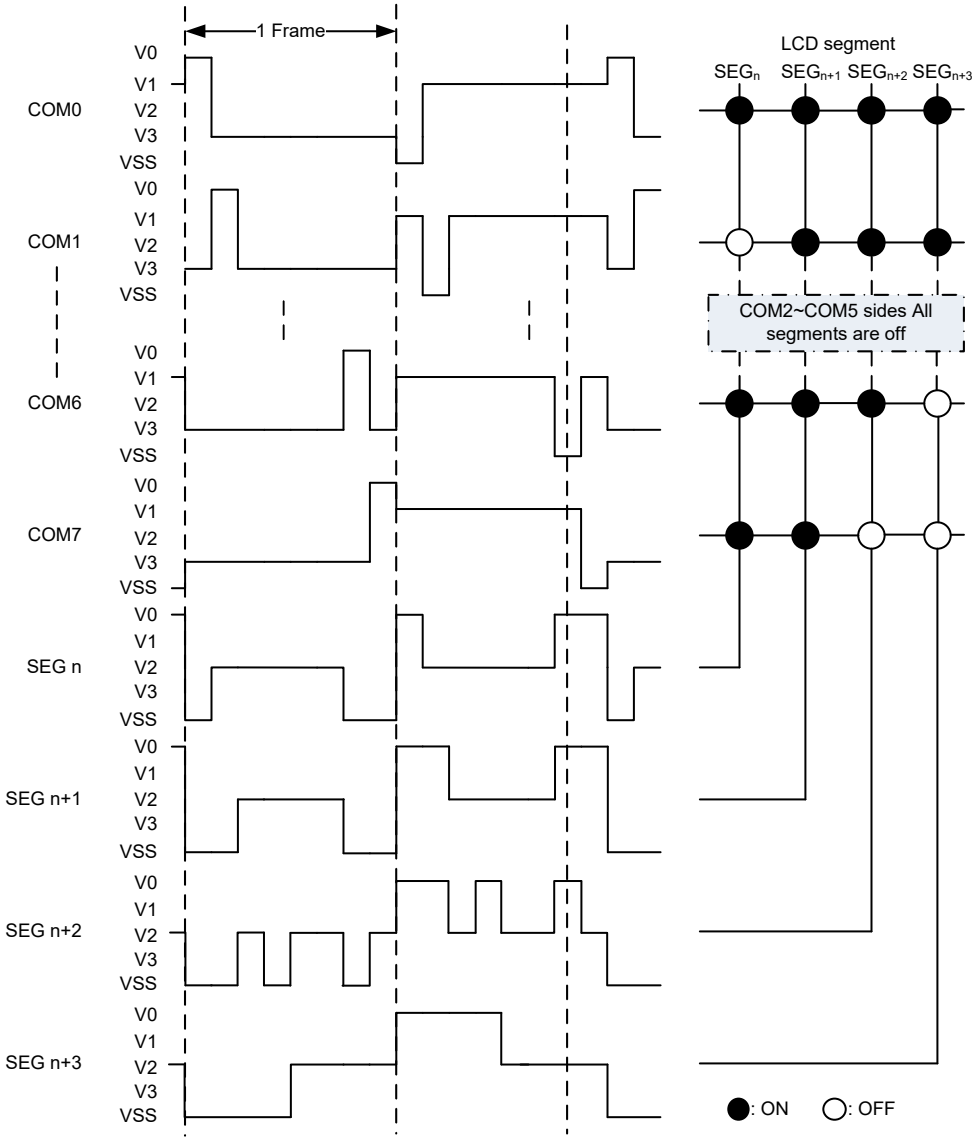
Duty=1/8, Bias=1/4, A Type Driving Waveform

The waveform and LCD display is shown below:



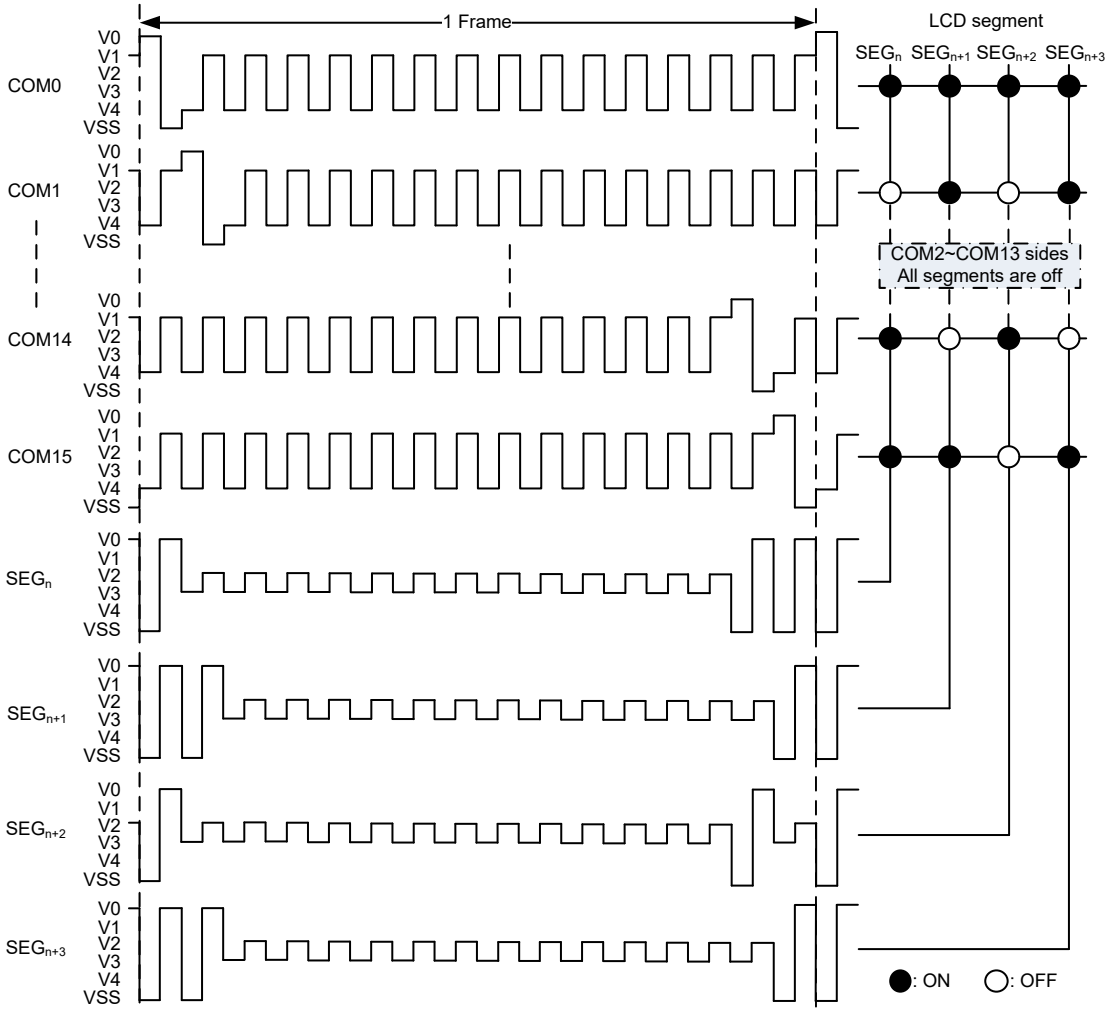
Duty=1/8, Bias=1/4, B Type Driving Waveform

The waveform and LCD display is shown below:



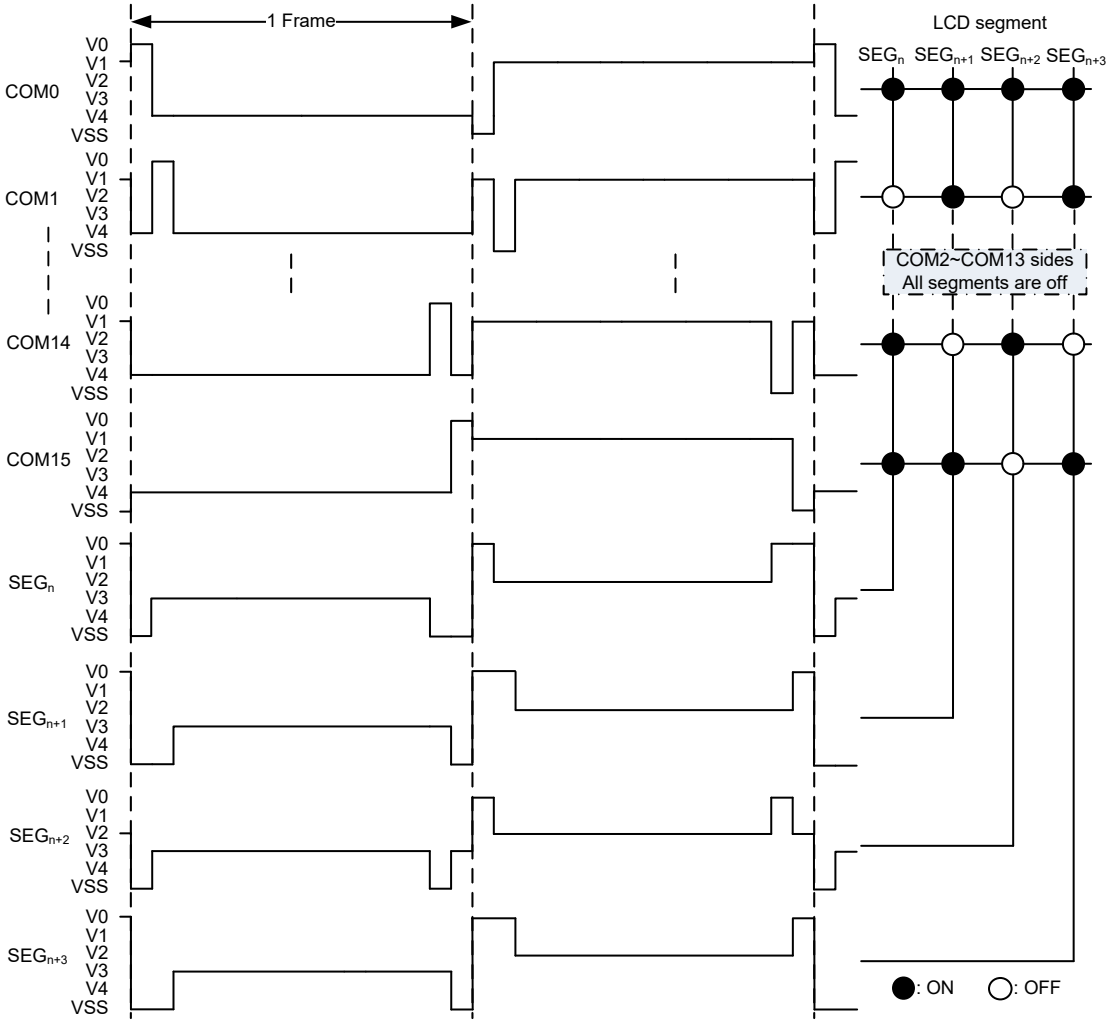
Duty=1/16, Bias=1/5, A Type Driving Waveform

The waveform and LCD display is shown below:



Duty=1/16, Bias=1/5, B type Driving Waveform

The waveform and LCD display is shown below:



Command Summary

Command Table

Command	R/W	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	Def.	Note
Software Reset	W	1	0	1	0	1	0	1	0	AAh	
LCD RAM R/W Command											
Write Display Data to Page 0	W	1	0	0	0	0	0	0	0	80h	
	W	A7	A6	A5	A4	A3	A2	A1	A0	00h	A[7:0]: Address Setting
	W	D7	D6	D5	D4	D3	D2	D1	D0	—	D[7:0]: Display Data
Read Display Data from Page 0	W	1	0	0	0	0	0	0	1	81h	
	W	A7	A6	A5	A4	A3	A2	A1	A0	00h	A[4:0]: Address Setting
	R	D7	D6	D5	D4	D3	D2	D1	D0	—	D[7:0]: Display Data
Write Display Data to Page 1	W	0	1	1	1	0	0	0	0	70h	
	W	A7	A6	A5	A4	A3	A2	A1	A0	00h	RAM Address Setting
	W	D7	D6	D5	D4	D3	D2	D1	D0	—	D[7:0]: Display Data
Read Display Data from Page 1	W	0	1	1	1	0	0	0	1	71h	
	W	A7	A6	A5	A4	A3	A2	A1	A0	00h	A[4:0]: Address Setting
	R	D7	D6	D5	D4	D3	D2	D1	D0	—	D[7:0]: Display Data
Page Configuration Mode	W	0	1	1	1	0	0	1	0	72h	
	W	X	X	X	X	X	X	X	PM	00h	PM: Page configuration
LCD Function Command											
Drive Mode Setting	W	1	0	0	0	0	0	1	0	82h	
	W	DT3	DT2	DT1	DT0	X	BS2	BS1	BS0	F7h	DT[3:0]: Duty setting BS[2:0]: Bias setting
Driving Waveform Setting	W	1	0	0	0	0	1	0	0	84h	
	W	X	X	X	X	X	X	X	DW	00h	DW: Driving waveform setting
System Mode Setting	W	1	0	0	0	0	1	1	0	86h	
	W	X	X	X	X	X	X	S	E	00h	S: Oscillator ON/OFF E: LCD Display ON/OFF
Frame Frequency Setting	W	1	0	0	0	1	0	0	0	88h	
	W	X	X	X	X	F3	F2	F1	F0	0Ah	F[3:0]: Frame Frequency Setting
Blinking Setting	W	1	0	0	0	1	0	1	0	8Ah	
	W	X	X	X	X	X	X	BK1	BK0	00h	BK[1:0]: Blink Frequency Setting
GPO Data R/W Command											
Write GPO Data	W	1	0	0	1	0	0	0	0	90h	
	W	X	X	X	X	D3	D2	D1	D0	—	D3~D0: GPO3~GPO0 Data
GPO/PWM Function Command											
Binary/PWM Select	W	1	0	0	1	0	0	1	0	92h	
	W	X	X	X	X	BPS3	BPS2	BPS1	BPS0	00h	BPS3~BPS0:Select GPOn as binary or PWM function
PWM Data R/W Command											
PWM Enable	W	1	0	1	1	0	0	0	0	B0h	
	W	X	X	X	X	PEN3	PEN2	PEN1	PEN0	00h	PEN3~PEN0: PWM Enable of GPO3~GPO0
Write PWM0 Data	W	1	0	1	1	0	0	1	0	B2h	
	W	X	X	D5	D4	D3	D2	D1	D0	—	D[5:0]:PWM data of GPO0

Command	R/W	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	Def.	Note
Write PWM1 Data	W	1	0	1	1	0	1	0	0	B4h	
	W	X	X	D5	D4	D3	D2	D1	D0	—	D[5:0]:PWM data of GPO1
Write PWM2 Data	W	1	0	1	1	0	1	1	0	B6h	
	W	X	X	D5	D4	D3	D2	D1	D0	—	D[5:0]:PWM data of GPO2
Write PWM3 Data	W	1	0	1	1	1	0	0	0	B8h	
	W	X	X	D5	D4	D3	D2	D1	D0	—	D[5:0]:PWM data of GPO3
Charge Pump Function Command											
Charge Pump Input Voltage Setting	W	1	1	0	0	0	0	0	0	C0h	
	W	VS	RE	X	RV4	RV3	RV2	RV1	RV0	00h	VS: Input Voltage Setting RE: Regulator Enable RV[4:0]: Regulator Voltage Setting
Charge Pump Control	W	1	1	0	0	0	0	1	0	C2h	
	W	CE	CR2	CR1	CR0	X	X	X	X	00h	CE: Charge Pump Enable CR[2:0]: Charge Pump ratio setting
LCD Bias Function Command											
LCD Bias Circuit Select	W	1	1	0	1	0	0	0	0	D0h	
	W	X	X	X	BV	X	X	BC1	BC0	00h	BV:LCD Bias Voltage Select BC[1:0]: LCD Bias Circuit Select
Contrast Adjustment	W	1	1	0	1	0	0	1	0	D2h	
	W	X	X	X	X	CA3	CA2	CA1	CA0	00h	CA[3:0]: Contrast Adjustment
Bias Resistor Set	W	1	1	0	1	0	1	0	0	D4h	
	W	X	X	X	X	X	X	BR1	BR0	02h	BR[1:0]: Bias Resistor Select

Note: 1. X: Don't care.
2. If programmed command data is not defined, the function will not be affected.

Software Reset Command

This command is used to initialise the device.

Command	R/W	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	Def.	Note
Software Reset	W	1	0	1	0	1	0	1	0	AAh	

Note:
- The status after software reset is the same as power-on reset. Refer to the power-on reset section for more information.

Write Display Data to Page 0 Command

This command is used to write the LCD display data to page 0.

Command	R/W	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	Def.	Note
Write Display Data to Page 0	W	1	0	0	0	0	0	0	0	80h	
	W	A7	A6	A5	A4	A3	A2	A1	A0	00h	A[7:0]: Address Setting
	W	D7	D6	D5	D4	D3	D2	D1	D0	—	D[7:0]: Display Data

Note:
- A[7:0]: LCD RAM address setting. The maximum address for each duty is shown in the "Display Memory – RAM Structure" section.
- D[7:0]: Display data. For the relationship between display and LCD display RAM, refer to the "Display Memory – RAM Structure" section.
- The input data is invalid if the LCD RAM address exceeds the address range.

Read Display Data from Page 0 Command

This command is used to read the LCD display data from page 0.

Command	R/W	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	Def.	Note
Read Display Data from Page 0	W	1	0	0	0	0	0	0	1	81h	
	W	A7	A6	A5	A4	A3	A2	A1	A0	00h	A[7:0]: Address Setting
	R	D7	D6	D5	D4	D3	D2	D1	D0	—	D[7:0]: Display Data

Note:
- A[7:0]: LCD RAM address setting. The maximum address for each duty is shown in the “Display Memory – RAM Structure” section.
- D[7:0]: Display data. For the relationship between display and LCD display RAM, refer to the “Display Memory – RAM Structure” section.

Write Display Data to Page 1 Command

This command is used to write the LCD display data to page 1.

Command	R/W	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	Def.	Note
Write Display Data to Page 1	W	0	1	1	1	0	0	0	0	70h	
	W	A7	A6	A5	A4	A3	A2	A1	A0	00h	A[7:0]: Address Setting
	W	D7	D6	D5	D4	D3	D2	D1	D0	—	D[7:0]: Display Data

Note:
- A[7:0]: LCD RAM address setting. The maximum address for each duty is shown in the “Display Memory – RAM Structure” section.
- D[7:0]: Display data. For the relationship between display and LCD display RAM, refer to the “Display Memory – RAM Structure” section.
- The input data is invalid if the LCD RAM address exceeds the address range.
- This command is valid when duty ≤ 1/8, it is forbidden to use when the duty is set to 1/9~1/16.

Read Display Data from Page 1 Command

This command is used to read the LCD display data from page 1.

Command	R/W	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	Def.	Note
Read Display Data from Page 1	W	0	1	1	1	0	0	0	1	71h	
	W	A7	A6	A5	A4	A3	A2	A1	A0	00h	A[7:0]: Address Setting
	R	D7	D6	D5	D4	D3	D2	D1	D0	—	D[7:0]: Display Data

Note:
- A[7:0]: LCD RAM address setting. The maximum address for each duty is shown in the “Display Memory – RAM Structure” section.
- D[7:0]: Display data. For the relationship between display and LCD display RAM, refer to the “Display Memory – RAM Structure” section.
- This command is valid when duty ≤ 1/8, it is forbidden to use when the duty is set to 1/9~1/16.

Page Configuration Mode Command

This command is used to set the RAM page.

Command	R/W	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	Def.	Note
Page Configuration Mode	W	0	1	1	1	0	0	1	0	72h	
	W	X	X	X	X	X	X	X	PM	00h	PM: Page configuration

Note:

PM	Page Configuration
0	Page0, the LCD display data is from page 0 RAM (default)
1	Page1, the LCD display data is from page 1 RAM

- This command is valid when duty ≤ 1/8, it is forbidden to use when the duty is set to 1/9~1/16.

Driver Mode Setting Command

This command is used to set the LCD duty and bias.

Command	R/W	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	Def.	Note
Drive Mode Setting	W	1	0	0	0	0	0	1	0	82h	
	W	DT3	DT2	DT1	DT0	X	BS2	BS1	BS0	F7h	DT[3:0]: Duty setting BS[2:0]: Bias setting

Note:

DT3	DT2	DT1	DT0	Duty Setting
0	0	0	0	Static
0	0	0	1	1/2
0	0	1	0	1/3
0	0	1	1	1/4
0	1	0	0	1/5
0	1	0	1	1/6
0	1	1	0	1/7
0	1	1	1	1/8

DT3	DT2	DT1	DT0	Duty Setting
1	0	0	0	1/9
1	0	0	1	1/10
1	0	1	0	1/11
1	0	1	1	1/12
1	1	0	0	1/13
1	1	0	1	1/14
1	1	1	0	1/15
1	1	1	1	1/16 (default)

BS2	BS1	BS0	Bias Setting
0	0	0	1/1
0	0	1	1/2
0	1	0	1/3
0	1	1	1/4
1	X	X	1/5 (default)

Driving Waveform Setting Command

This command is used to set the LCD driving waveform.

Command	R/W	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	Def.	Note
Drive Waveform Setting	W	1	0	0	0	0	1	0	0	84h	
	W	X	X	X	X	X	X	X	DW	00h	DW: Driving Waveform setting

Note:

DW	Driving Waveform
0	A type (default)
1	B type

System Mode Setting Command

This command is used to set the internal oscillator on/off and display on/off.

Command	R/W	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	Def.	Note
System Mode Setting	W	1	0	0	0	0	1	1	0	86h	
	W	X	X	X	X	X	X	S	E	00h	S: Oscillator ON/OFF E: LCD Display ON/OFF

Note:

S	E	Internal Oscillator	LCD Display
0	X	off (default)	off
1	0	on	off
1	1	on	on

- It is strongly recommended that the LCD display should first be switched off before the “S” bit is cleared to 0. Otherwise, the LCD display will be turned on automatically when the “S” bit is set to 1.
- When the “S” bit is cleared to “0”, the internal oscillator is off, the device status is shown as follows:
  - The Internal oscillator and LCD display are in an off state.
  - All commons and segments are set to VSS.
  - The GPO function is not affected.
  - The PWM function and outputs are disabled.
  - Set RE=“0” and CE=“0” to reduce power consumption.
- When the LCD display is OFF, the commons and segments will be set to VSS.
- The “E” bit only controls the LCD display, the GPO and PWM function are not affected.

Frame Frequency Setting Command

This command is used to set the LCD frame frequency.

Command	R/W	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	Def.	Note
Frame Frequency Setting	W	1	0	0	0	1	0	0	0	88h	
	W	X	X	X	X	F3	F2	F1	F0	0Ah	F[3:0]: Frame Frequency Setting

Note:

- The frame frequency for each duty setting is shown below.

F3	F2	F1	F0	Frame Frequency (Hz)															duty
				Static	1/2	1/3	1/4	1/5	1/6	1/7	1/8	1/9	1/10	1/11	1/12	1/13	1/14	1/15	1/16	
0	0	0	0	50	50	44	50	80	67	57	50	44	40	73	67	62	57	53	50	
0	0	0	1	60	60	53	60	96	80	69	60	53	48	87	80	74	69	64	60	
0	0	1	0	70	70	62	70	112	93	80	70	62	56	102	93	86	80	75	70	
0	0	1	1	80	80	71	80	128	107	91	80	71	64	116	107	98	91	85	80	
0	1	0	0	90	90	80	90	144	120	103	90	80	72	131	120	111	103	96	90	
0	1	0	1	100	100	89	100	160	133	114	100	89	80	145	133	123	114	107	100	
0	1	1	0	120	120	107	120	192	160	137	120	107	96	175	160	148	137	128	120	
0	1	1	1	140	140	124	140	224	187	160	140	124	112	204	187	172	160	149	140	
1	0	0	0	160	160	142	160	256	213	183	160	142	128	233	213	197	183	171	160	
1	0	0	1	180	180	160	180	288	240	206	180	160	144	262	240	222	206	192	180	
1	0	1	0	200	200	178	200	320	267	229	200	178	160	291	267	246	229	213	200	default
1	0	1	1	220	220	196	220	352	293	251	220	196	176	320	293	271	251	235	220	
1	1	0	0	240	240	213	240	384	320	274	240	213	192	349	320	295	274	256	240	
1	1	0	1	260	260	231	260	416	347	297	260	231	208	378	347	320	297	277	260	
1	1	1	0	280	280	249	280	448	373	320	280	249	224	407	373	345	320	299	280	
1	1	1	1	300	300	267	300	480	400	343	300	267	240	436	400	369	343	320	300	

- The PWM frame frequency depends on the frame frequency setting as shown in the following table.

F3	F2	F1	F0	PWM frame frequency (Hz)
0	0	0	0	800
0	0	0	1	960
0	0	1	0	1120
0	0	1	1	1280
0	1	0	0	1440
0	1	0	1	1600
0	1	1	0	1920
0	1	1	1	2240
1	0	0	0	2560
1	0	0	1	2880
1	0	1	0	3200 (default)
1	0	1	1	3520
1	1	0	0	3840
1	1	0	1	4160
1	1	1	0	4480
1	1	1	1	4800

Blinking Frequency Setting Command

This command is used to set the LCD blinking frequency.

Command	R/W	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	Def.	Note
Blinking Setting	W	1	0	0	0	1	0	1	0	8Ah	
	W	X	X	X	X	X	X	BK1	BK0	00h	BK[1:0]: Blink Frequency Setting

Note:

BK1	BK0	Blinking Frequency Setting
0	0	off (default)
0	1	2Hz
1	0	1Hz
1	1	0.5Hz

- The blinking frequency values are for reference only. There is a little difference at different duty and frame frequency setting.

Write GPO Data Command

This command is used to write GPO data.

Command	R/W	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	Def.	Note
Write GPO Data	W	1	0	0	1	0	0	0	0	90h	
	W	X	X	X	X	D3	D2	D1	D0	—	D3~D0: GPO3~GPO0 Data

Note:
- D3~D0: GPO3~GPO0 data

Bit	Data to the Corresponding GPO Pin
D3	GPO3
D2	GPO2
D1	GPO1
D0	GPO0

Binary/PWM Function Select Command

This command is used to select whether the GPO output is binary or PWM function.

Command	R/W	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	Def.	Note
Binary/PWM Select	W	1	0	0	1	0	0	1	0	92h	
	W	X	X	X	X	BPS3	BPS2	BPS1	BPS0	00h	BPS3~BPS0: Select GPOn is binary or PWM function

Note:
- BPS3~BPS0: Select the GPO output is binary or PWM function in GPO output

BPSn	GPOn or PWMn Output Select
0	GPO output
1	PWM output

Note: n=0~3

Bit	Bit to the corresponding GPO pin
BPS3	GPO3
BPS2	GPO2
BPS1	GPO1
BPS0	GPO0

PWM Enable Command

This command is used to enable the GPO PWM output.

Command	R/W	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	Def.	Note
PWM Enable	W	1	0	0	1	1	0	0	0	B0h	
	W	X	X	X	X	PEN3	PEN2	PEN1	PEN0	00h	PEN3~PEN0: GPOn PWM output enable

Note:

PENn	GPOn PWM Output Enable
0	PWM output disable. GPOn output is in a low level (default)
1	PWM output enable. GPOn output duty is set using PWM data command

Note: n=0~3

Bit	Bit to the Corresponding GPO Pin
PEN3	GPO3
PEN2	GPO2
PEN1	GPO1
PEN0	GPO0

Write PWM Data Command

This command is used to write the PWM data to GPO0~GPO3.

Command	R/W	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	Def.	Note
Write PWM Data to GPO0	W	1	0	0	1	1	0	0	0	B2h	
	W	X	X	D5	D4	D3	D2	D1	D0	00h	PWM data of GPO0
Write PWM Data to GPO1	W	1	0	0	1	1	0	0	0	B4h	
	W	X	X	D5	D4	D3	D2	D1	D0	00h	PWM data of GPO1
Write PWM Data to GPO2	W	1	0	0	1	1	0	0	0	B6h	
	W	X	X	D5	D4	D3	D2	D1	D0	00h	PWM data of GPO2
Write PWM Data to GPO3	W	1	0	0	1	1	0	0	0	B8h	
	W	X	X	D5	D4	D3	D2	D1	D0	00h	PWM data of GPO3

Note:
● D[5:0]: PWM data. The relationship between PWM data and PWM duty is shown below.

D[5:0]	PWM Duty
000000	1/64
000001	2/64
000010	3/64
:	:
011010	27/64
011011	28/64
011100	29/64
:	:
111101	62/64
111110	63/64
111111	64/64

Charge Pump Input Voltage Setting Command

This command is used to set the charge pump input voltage.

Command	R/W	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	Def.	Note
Charge Pump Input Voltage Setting	W	1	1	0	0	0	0	0	0	C0h	
	W	VS	RE	X	RV4	RV3	RV2	RV1	RV0	00h	VS: Input Voltage Setting RE: Regulator Enable RV[4:0]: Regulator Voltage Setting

Note:

● VS: Charge pump input voltage source setting

VS	Charge Pump Input Voltage Setting
0	V_{DD} (default)
1	Internal Regulator

● RE: Internal regulator enable

RE	Regulator Enable
0	Disable (default)
1	Enable

● RV[4:0]: Internal regulator voltage output setting

Note that in order to ensure the regulator normal operation, the V_{DD} should satisfy the condition:

$V_{DD} \geq$ Regulator Voltage + 0.2V

RV4	RV3	RV2	RV1	RV0	Regulator Voltage (V)
0	0	0	0	0	1.0 (default)
0	0	0	0	1	1.1
0	0	0	1	0	1.2
0	0	0	1	1	1.3
0	0	1	0	0	1.4
0	0	1	0	1	1.5
0	0	1	1	0	1.6
0	0	1	1	1	1.7
0	1	0	0	0	1.8
0	1	0	0	1	1.9
0	1	0	1	0	2.0
0	1	0	1	1	2.1
0	1	1	0	0	2.2
0	1	1	0	1	2.3
0	1	1	1	0	2.4
0	1	1	1	1	2.5

RV4	RV3	RV2	RV1	RV0	Regulator Voltage (V)
1	0	0	0	0	2.6
1	0	0	0	1	2.7
1	0	0	1	0	2.8
1	0	0	1	1	2.9
1	0	1	0	0	3.0
1	0	1	0	1	3.1
1	0	1	1	0	3.2
1	0	1	1	1	3.3
1	1	0	0	0	3.4
1	1	0	0	1	3.5
1	1	0	1	0	3.6
1	1	0	1	1	3.7
1	1	1	0	0	3.8
1	1	1	0	1	3.9
1	1	1	1	0	4.0
1	1	1	1	1	4.1

Charge Pump Control Command

This command is used to control the charge pump.

Command	R/W	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	Def.	Note
Charge Pump Control	W	1	1	0	0	0	0	1	0	C2h	
	W	CE	CR2	CR1	CR0	X	X	X	X	00h	CE: Charge pump enable CR[2:0]: Charge Pump ratio setting

Note:
● CE: Charge pump enable

CE	Charge Pump Control
0	Charge Pump Disable (default)
1	Charge Pump Enable

● CR[2:0]: Charge pump ratio setting
Refer to the “Charge Pump” section to obtain the charge pump configuration for each ratio.

CR2	CR1	CR0	Charge Pump Ratio
0	0	0	Charge Pump Input Voltage (default)
0	0	1	×2
0	1	0	×3
0	1	1	×4
1	X	X	×5

LCD Bias Circuit Select Command

This command is used to select the LCD bias circuit.

Command	R/W	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	Def.	Note
LCD Bias Circuit Select	W	1	1	0	1	0	0	0	0	D0h	
	W	X	X	X	BV	X	X	BC1	BC0	00h	BV: V_{LCD} select BC[1:0]: LCD Bias Circuit Select

Note:
● BV: V_{LCD} select

BV	V_{LCD} Select
0	V_{LCD} is supplied from charge pump (default)
1	V_{LCD} is supplied from external power

● BC[1:0]: LCD Bias Circuit Select

BC1	BC0	LCD Bias Circuit Select
0	0	Disable (default)
0	1	Charge Pump
1	0	Invalid, cannot be used.
1	1	Resistor Divider

Contrast Adjustment Command

This command is used to adjust the contrast.

Command	R/W	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	Def.	Note
Contrast Adjustment	W	1	1	0	1	0	0	1	0	D2h	
	W	X	X	X	X	CA3	CA2	CA1	CA0	00h	CA[3:0]: Contrast adjustment

Note:
- CA[3:0]: Contrast adjustment bit, when LCD bias circuit is set to resistor divider.
- Refer to the "Contrast Adjustment "section for the adjustment value.

Bias Resistor Set Command

This command is used to set the bias resistor value.

Command	R/W	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	Def.	Note
Bias Resistor Set	W	1	1	0	1	0	1	0	0	D4h	
	W	X	X	X	X	X	X	BR1	BR0	02h	BR[1:0]: Bias resistor set

Note:
- BR[1:0]: Bias resistor value. This command is valid when the LCD bias circuit is set to resistor divider.

BR1	BR0	Resistor Value
0	0	4kΩ
0	1	8kΩ
1	X	16kΩ (default)

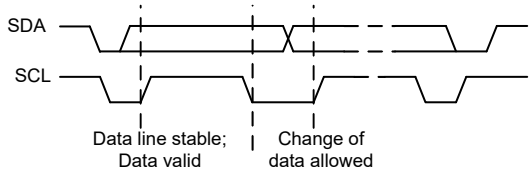
Serial Interface

I²C Serial Interface

The device includes an I²C serial interface. The I²C bus is a bidirectional, two-line communication link between different ICs or modules. The two lines are a serial data line, SDA, and a serial clock line, SCL. Both lines are connected to a positive supply via a pull-up resistor with a typical value of 4.7kΩ. When the bus is free, both lines are high. The output stages of any devices connected to the bus must have open-drain or open-collector types in order to implement a wired-or function. Data transfer is initiated only when the bus is not busy.

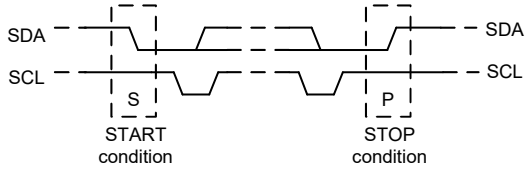
Data Validity

The data on the SDA line must be stable during the clock high period. The high or low state of the data line can only change when the clock signal on the SCL line is low as shown in the accompanying diagram.



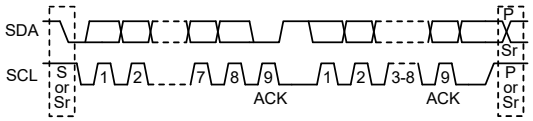
START and STOP Conditions

- A high to low transition on the SDA line while SCL is high defines a START condition.
- A low to high transition on the SDA line while SCL is high defines a STOP condition.
- START and STOP conditions are always generated by the master. The bus is considered to be busy after the START condition. The bus is considered to be free again a certain time after the STOP condition.
- The bus remains busy if a repeated START (Sr) is generated instead of a STOP condition. The START (S) and repeated START (Sr) conditions are functionally identical.



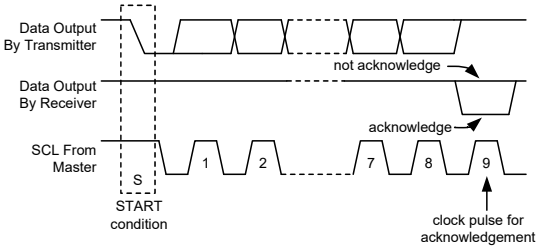
Byte Format

Every byte put on the SDA line must be 8 bits long. The number of bytes that can be transmitted per transfer is unrestricted. Each byte has to be followed by an acknowledge bit. Data is transferred with the most significant bit (MSB) first.



Acknowledge

- Each bytes of eight bit length is followed by one acknowledge bit. This acknowledge bit is a low level placed on the bus by the receiver. The master generates an extra acknowledge related clock pulse.
- A slave receiver which is addressed must generate an acknowledge, ACK, after the reception of each byte.
- The device that provides an acknowledge must pull down the SDA line during the acknowledge clock pulse so that it remains at a stable low level during the high period of this clock pulse.
- A master receiver must signal an end of data to the slave by generating a not-acknowledge, NACK, bit on the last byte that has been clocked out of the slave. In this case, the master receiver must leave the data line high during the 9th pulse so as to not acknowledge. The master will generate a STOP or a repeated START condition.



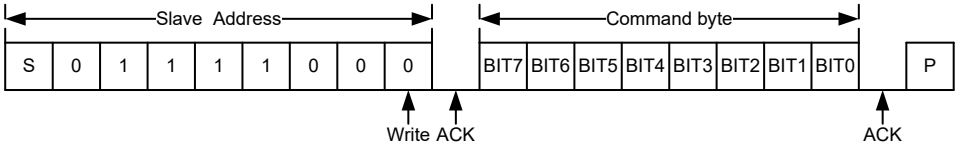
Slave Addressing

- The slave address byte is the first byte received following the START condition from the master device. The first seven bits of the first byte make up the slave address. The eighth bit defines whether a read or write operation is to be performed. When the R/W bit is "1", then a read operation is selected. A "0" selects a write operation.
- The address bits are "0111100". When an address byte is sent, the device compares the first seven bits after the START condition. If they match, the device outputs an Acknowledge on the SDA line.

Write Operation

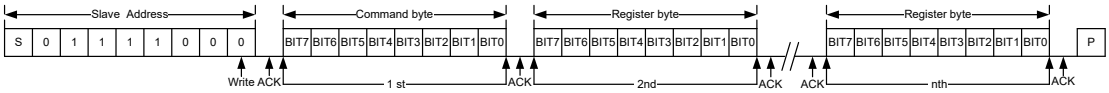
Single Command Type

A single command write operation requires a START condition, a slave address with an R/W bit, a command byte and a STOP condition.



Compound Command Type

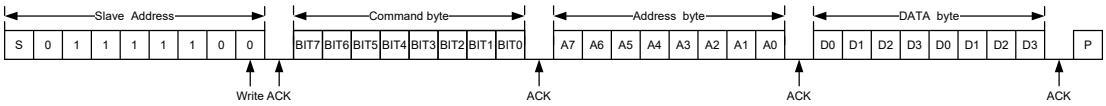
A compound command write operation requires a START condition, a slave address with an R/W bit, a command byte, one or more register byte which depends upon the command format and a STOP condition.



Single Display RAM Data Byte

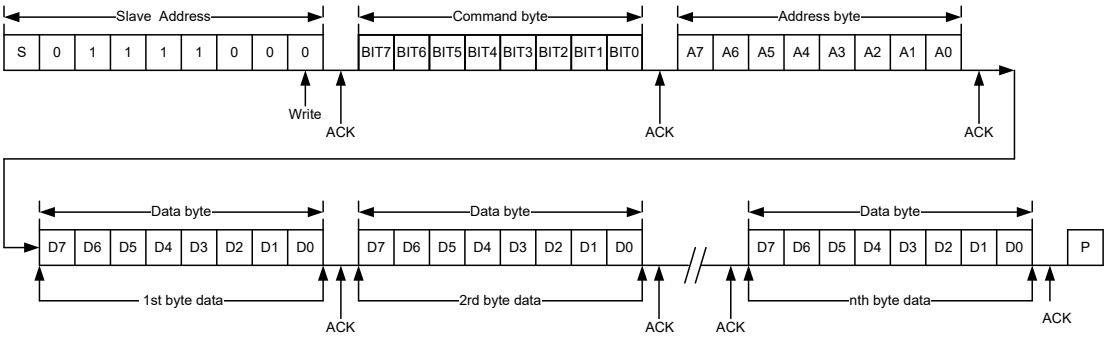
A single display RAM data byte write operation requires a START condition, a slave address with an R/W bit, a write display command byte, a valid address byte, a DATA byte and a STOP condition.

If the address byte is greater than the limit value, the data will be invalid. The address byte range is described in the "Display Memory – RAM Structure" section.



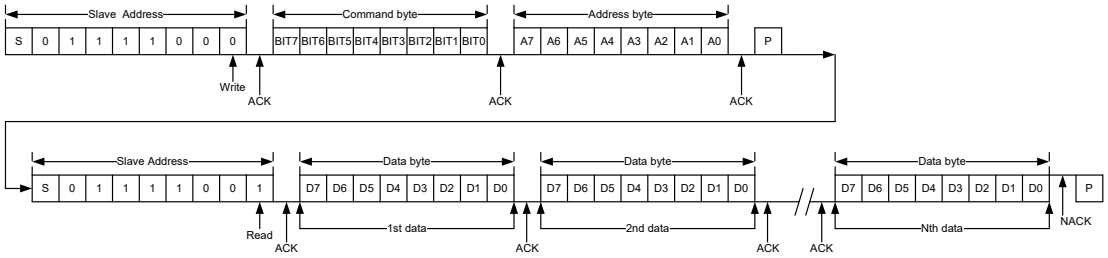
Display RAM Page Write Operation

Following a START condition the slave address with the R/W bit is placed on the bus along with the write display data command byte and the specified address byte of which the contents are written to the internal address pointer. The data to be written to the memory will be transmitted next and then the internal address pointer will be incremented by 1 to indicate the next memory address location after the reception of an acknowledge clock pulse. After the internal address point reaches the maximum memory address, the address pointer will be reset to 00h. The address pointer range is described in the "Display Memory – RAM Structure" section.



Read Operation

In this mode, the master reads the device data after setting the slave address. Following the R/W bit (="0") is an acknowledge bit, a command byte and the address byte which is written to the internal address pointer. After the start address of the Read Operation has been configured, another START condition and the slave address transferred on the bus followed by the R/W bit ("1"). Then the MSB of the data which was addressed is transmitted first on the I^2C bus. The address pointer is only incremented by 1 after the reception of an acknowledge clock. That means that if the device is configured to transmit the data at the address of A_{N+1}, the master will read and acknowledge the transferred new data byte and the address pointer is incremented to A_{N+2}. After the internal address pointer reaches the maximum memory address, the address pointer will be reset to 00h. The address point range is described in the "Display Memory – RAM Structure" section.



Display RAM Data Read Operation

SPI Serial Interface

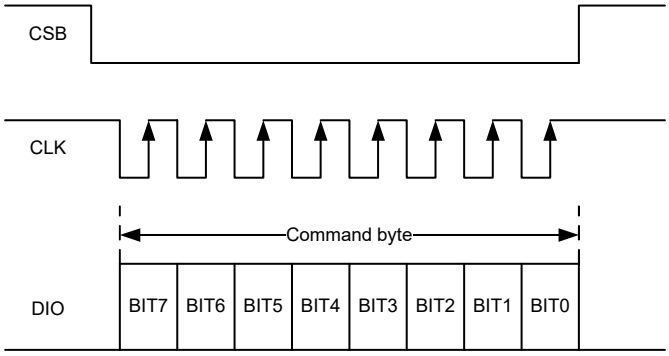
The device also includes a 3-wire SPI serial interface. The SPI operations are described as follows:

- The CSB pin is used to activate the data transfer. When the CSB pin is at a high level, the SPI operation will be reset and stopped. If the CSB pin changes state from high to low, data transmission will start.
- The data is transferred from the MSB of each byte (MSB First), and is shifted into the shift register at the CLK rising edge.
- The input data is automatically latched into the internal register for each 8-bit input data after the CSB pin goes low.
- For read operations, the MCU should assert a high pulse on the CSB pin to change the data transfer direction from input mode to output mode on the DIO pin after sending the command byte and the address byte. If the MCU sets the CSB pin to a high level again after receiving the output data, the data direction on the DIO pin will be changed into input mode and the read operation will end.
- For a read operation the data is output on the DIO pin at the CLK falling edge.

Write Operation

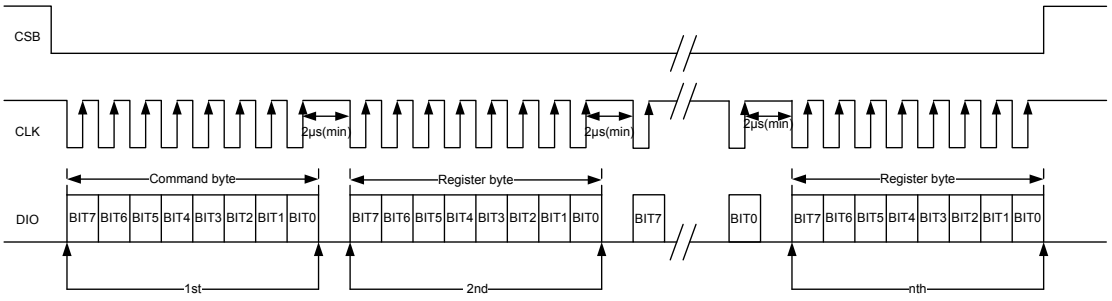
Single Command Type

A single command write operation is activated by the CSB pin going low. The 8-bit command byte is shifted from the MSB into the shift register at each CLK rising edge.



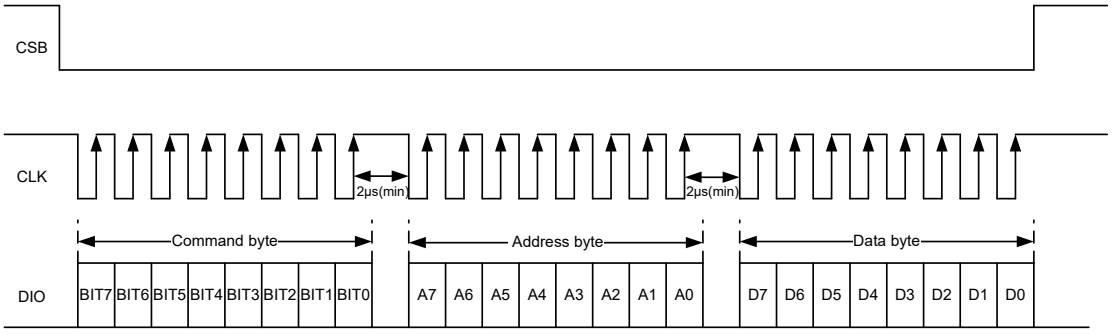
Compound Command Type

A compound command write operation is activated by the CSB pin going low. The 8-bit command byte is first shifted into the shift register followed by one or more 8-bit register byte which depends upon the command format. Note that the CLK high pulse width, after the command byte has been shifted in, must remain at this level. The 8-bit command byte is shifted from the MSB into the shift register at each CLK rising edge.



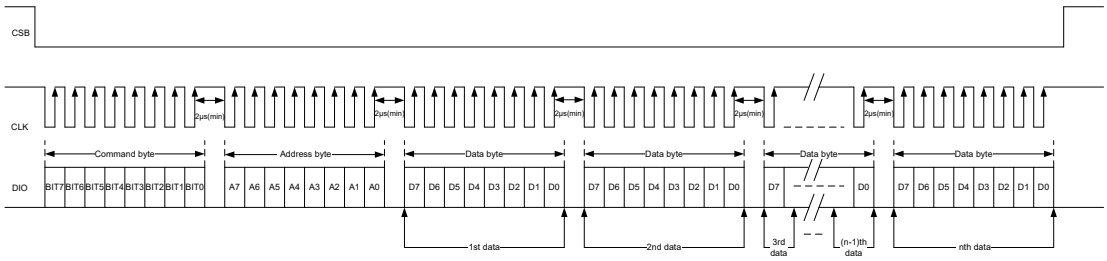
Single Display RAM Data Byte

The single display RAM data write operation consists of a write display data command byte, an address byte and a data byte.



Display RAM Page Write Operation

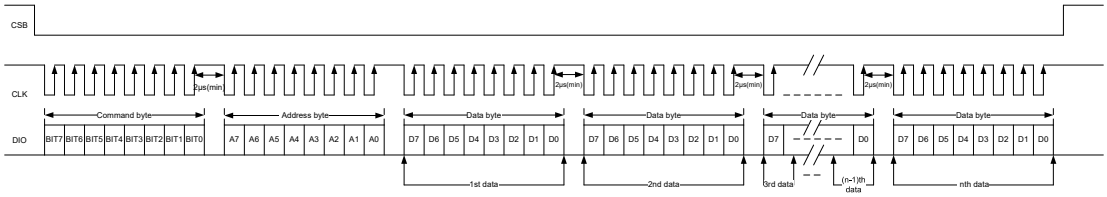
The display RAM Page write operation consists of a write display data command, an address byte of which the contents are written to the internal address pointer followed by N bytes of written data. The data to be written to the memory will be transmitted next and then the internal address pointer will be automatically incremented by 1 to indicate the next memory address location. After the internal address point reaches the maximum memory address, the address pointer will be reset to 00h. The address byte range is described in the "Display Memory – RAM Structure" section.



Read Operation – Display RAM

In this mode, the master reads the device data after sending the read display data command byte and the address byte when the CSB pin changes state from high to low. Following the read display data command byte and the address byte which is written to the internal address pointer. After the start address of the Read Operation has been configured, the MSB of the data which was addressed is transmitted first on the SPI bus. The address pointer is only incremented by 1 after the reception of each data byte. That means that if the device is configured to transmit the data at the address of A_{N+1}, the master will read the transferred data byte and the address pointer will be incremented to A_{N+2}. After the internal address pointer reaches the maximum memory address, the address pointer will be reset to 00h. The address point range is described in the "Display Memory – RAM Structure" section.

This cycle of reading consecutive addresses will continue until master pulls the CSB line to a high level to terminate the data transfer.

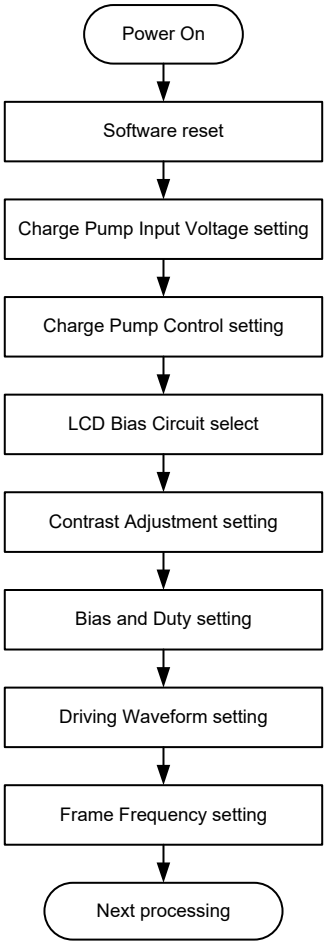


Display RAM Data Read Operation

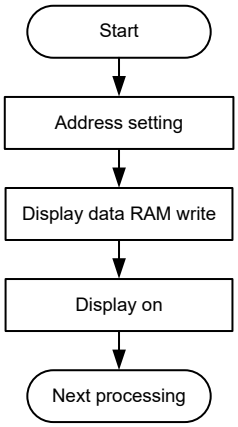
Operation Flowchart

Access procedures are illustrated below using flowcharts.

Initialisation



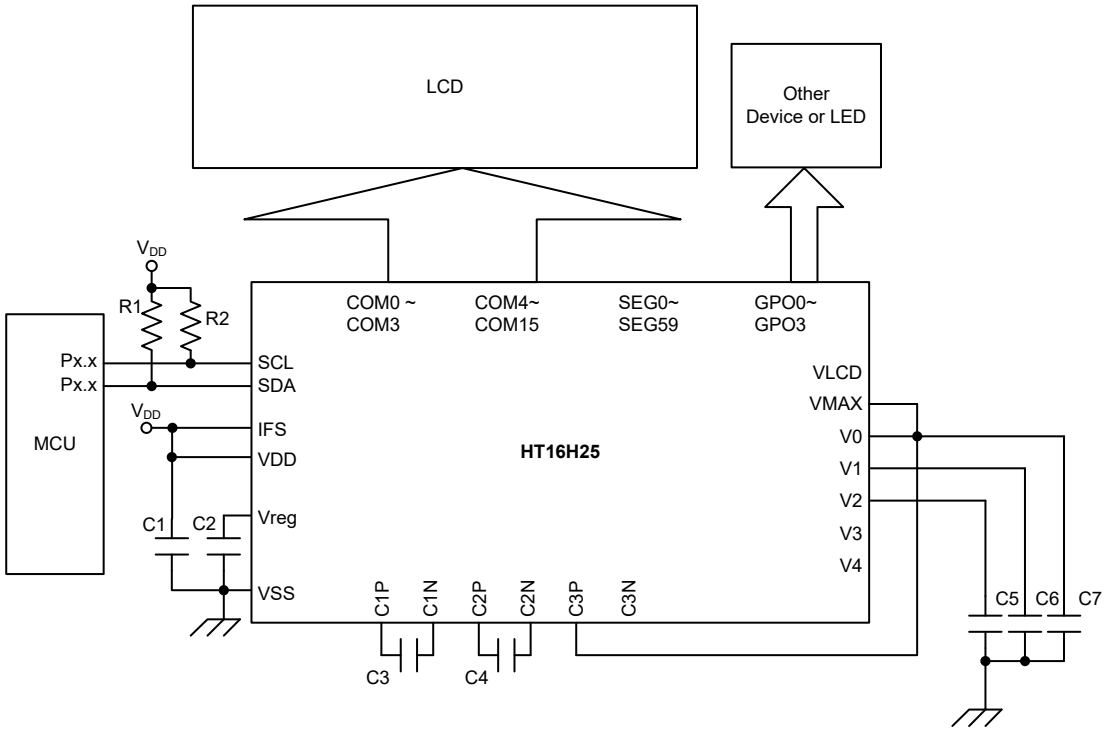
Display Data Write (Address Setting)



Application Circuits

Application examples for the specified conditions:

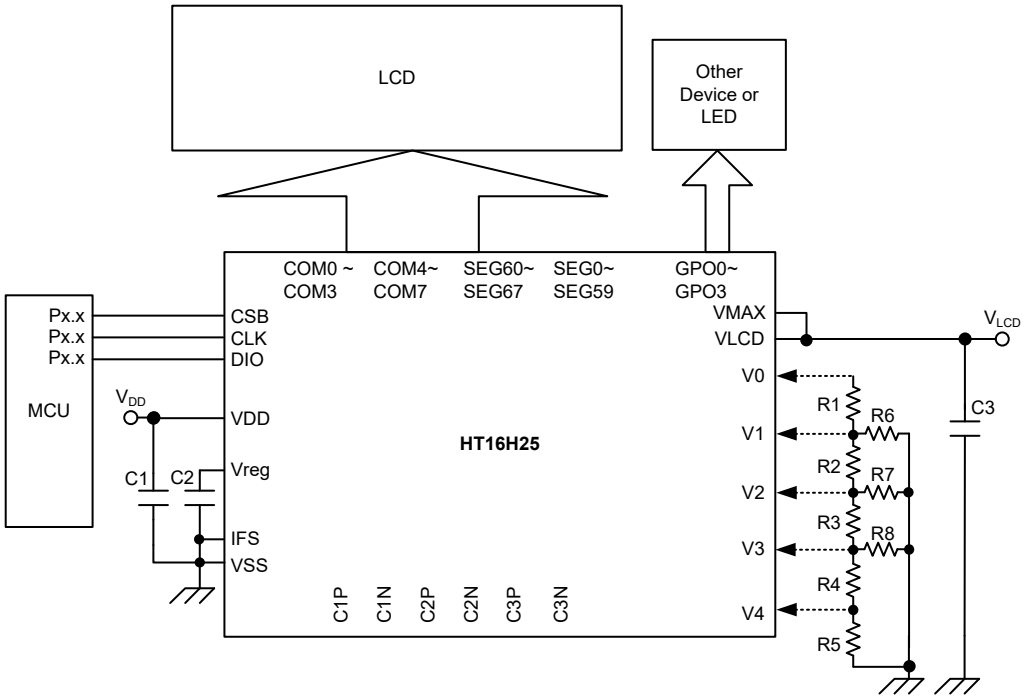
- 1/16 duty, V_{LCD} is supplied from charge pump, charge pump=×3, $V_{LCD} > V_{DD}$
  LCD bias circuit=charge pump, I^2C Interface



Note: C1=C3=C4=C5=C6=C7=0.1μF, C2=1μF, R1=R2=4.7kΩ.

- 1/8 duty, V_{LCD} is supplied from VLCD pin, $V_{LCD} > V_{DD}$

  LCD bias circuit=resistor divider, SPI 3-wire Interface



Note: 1. C1=C3=0.1μF, C2=1μF

2. Users can connect an external resistor divider to V0~V4 when driving the large panel.

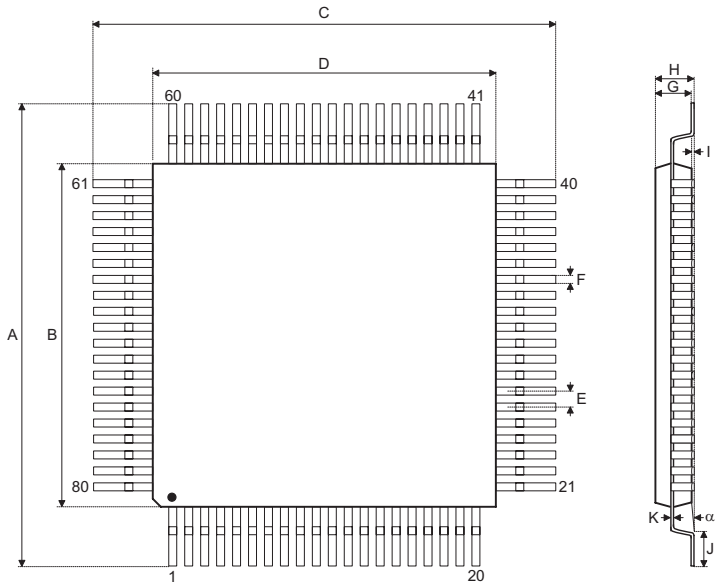
Package Information

Note that the package information provided here is for consultation purposes only. As this information may be updated at regular intervals users are reminded to consult the Holtek website for the latest version of the Package/Carton Information.

Additional supplementary information with regard to packaging is listed below. Click on the relevant section to be transferred to the relevant website page.

- Package Information (include Outline Dimensions, Product Tape and Reel Specifications)
- The Operation Instruction of Packing Materials
- Carton information

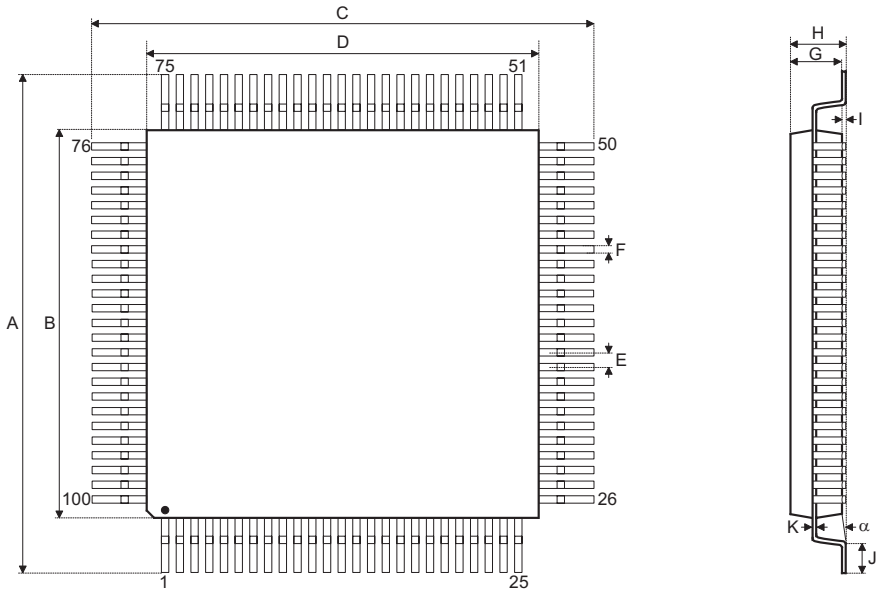
80-pin LQFP (10mm×10mm) Outline Dimensions



Symbol	Dimensions in inch		
	Min.	Nom.	Max.
A		0.472 BSC	
B		0.394 BSC	
C		0.472 BSC	
D		0.394 BSC	
E		0.016 BSC	
F	0.005	0.007	0.009
G	0.053	0.055	0.057
H	—	—	0.063
I	0.002	—	0.006
J	0.018	0.024	0.030
K	0.004	—	0.008
α	0°	—	7°

Symbol	Dimensions in mm		
	Min.	Nom.	Max.
A		12.00 BSC	
B		10.00 BSC	
C		12.00 BSC	
D		10.00 BSC	
E		0.40 BSC	
F	0.13	0.18	0.23
G	1.35	1.40	1.45
H	—	—	1.60
I	0.05	—	0.15
J	0.45	0.60	0.75
K	0.09	—	0.20
α	0°	—	7°

100-pin LQFP (14mm×14mm) Outline Dimensions



Symbol	Dimensions in inch		
	Min.	Nom.	Max.
A		0.630 BSC	
B		0.551 BSC	
C		0.630 BSC	
D		0.551 BSC	
E		0.020 BSC	
F	0.007	0.009	0.011
G	0.053	0.055	0.057
H	—	—	0.063
I	0.002	—	0.006
J	0.018	0.024	0.030
K	0.004	—	0.008
α	0°	—	7°

Symbol	Dimensions in mm		
	Min.	Nom.	Max.
A		16.00 BSC	
B		14.00 BSC	
C		16.00 BSC	
D		14.00 BSC	
E		0.50 BSC	
F	0.17	0.22	0.27
G	1.35	1.40	1.45
H	—	—	1.60
I	0.05	—	0.15
J	0.45	0.60	0.75
K	0.09	—	0.20
α	0°	—	7°