



# DATA SHEET

( DOC No. HX8347-G(T)-DS )

## HX8347-G(T)

240RGB x 320 dot, 262K color,  
with internal GRAM,  
TFT Mobile Single Chip Driver  
*Version 01 February, 2010*

# HX8347-G(T)

240RGB x 320 dot, 262K color, with internal GRAM, TFT Mobile Single Chip Driver



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» **HX8347-G(T)**

240RGB x 320 dot, 262K color, with internal  
GRAM, TFT Mobile Single Chip Driver



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**Version 01**

February, 2010

## 1. General Description

This document describes HX8347-G 240RGBx320 dots resolution driving controller. The HX8347-G is designed to provide a single-chip solution that combines a gate driver, a source driver, power supply circuit for 262,144 colors to drive a TFT panel with 240RGBx320 dots at maximum.

The HX8347-G can be operated in low-voltage (1.4V) condition for the interface and integrated internal boosters that produce the liquid crystal voltage, breeder resistance and the voltage follower circuit for liquid crystal driver. In addition, The HX8347-G also supports various functions to reduce the power consumption of a LCD system via software control.

The HX8347-G supports two interface groups: Command-Parameter interface group, Register-Content interface group. The interface groups are selected by the external pin IFSEL setting. This manual description focuses on Register-Content interface group. About the Command-Parameter interface group, please refer to the HX8347-G (N) datasheet for detail.

The HX8347-G is suitable for any small portable battery-driven and long-term driving products, such as small PDAs, digital cellular phones and bi-directional pagers.

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## 2. Features

### 2.1 Display

- Resolution:
  - 240(H) x RGB(H) x 320(V)
- Display Color modes
  - Normal Display Mode On
    1. System Interface Circuit
      - a. Full color mode:
        - 262k colours (18bit 6(R):6(G):6(B))
      - b. Reduce color mode:
        - 65k colours (16bit 5(R):6(G):5(B))
        - 4096 colours(12bit 4(R):4(G):4(B))
    2. RGB Interface Circuit
      - a. 65,536(R(5),G(6),B(5)) colors
      - b. 262,144(R(6),G(6),B(6)) colors
  - Idle Mode On
    - 8 (R(1),G(1),B(1)) colors

### 2.2 Display Module

- Frame Memory area 240 (H) x 320 (V) x 18 bit
- On module DC/DC converter
- DDVDH = 5.0 V for two time pump (Power supply for driver circuit range)
- DDVDH = 6.1 V for three time pump (Power supply for driver circuit range)
- VREG1 = 3.3V to 5.8V (Source output voltage range)
- VGH = +9.0 to +16.5V (Positive Gate output voltage range)
- VGL = -6.0 to -13.5V (Negative Gate output voltage range)
- VCOMH = 2.5V to 5.8V, 15mv/step (Common electrode output high voltage)
- VCOML = -2.5V to 0.0V, 15mv/step (Common electrode output low voltage)

### 2.3 Display Control Interface

- Display Interface types supported
  - System interface:
    1. 8-/9-/16-/18-bit parallel bus system interface
    2. 3-/4-wire serial bus system interface
  - RGB interface:
    1. 6-/16-/18-bit RGB interface
- Color modes
  - 12 bit/pixel: R(4), G(4), B(4)
  - 16 bit/pixel: R(5), G(6), B(5)
  - 18 bit/pixel: R(6), G(6), B(6)



**2.4 Input power**

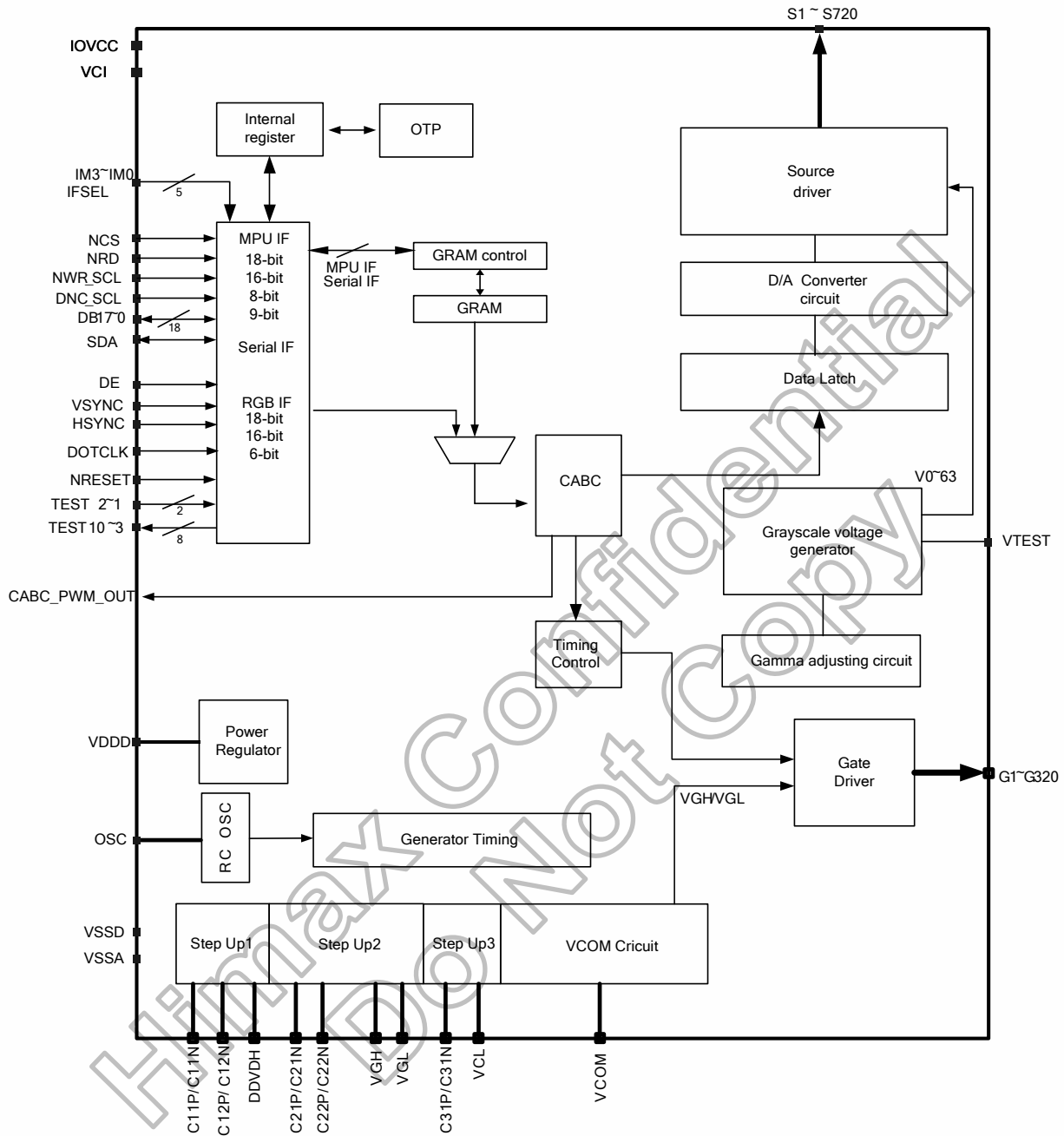
- Logic power supply (IOVCC): 1.65V ~ 3.3V
- Analog power supply (VCI): 2.5V ~ 3.3V
- OTP programming voltage (VPP): 6.5V  $\pm$  0.2V

**2.5 Miscellaneous**

- Low power consumption, suitable for battery operated systems
- Image sticking eliminated function
- CMOS compatible inputs
- Optimized layout for COG assembly
- Proprietary multi phase driving for lower power consumption
- Support external VDDD for lower power consumption (such as 1.8 volts input)
- Support 1~7 Line inversion or Frame inversion
- Support Area scrolling
- Support Partial display mode
- Support Deep standby mode
- Support normal black/normal white LCD
- Support wide view angle display
- On-chip OTP (One-time-programming) and MTP(three-time-programming for some register) non-volatile memory
- Support Content Adaptive Brightness Control(CABC) function
- Support Digital Gamma function
- Operating temperature range : -40°C ~ 85°C

### 3. Block Diagram

#### 3.1 Block diagram



## 3.2 Pin description

| Interface Logic Pin   |     |            |                         |  |                                   |
|---|-----|------------|-------------------------|--|-----------------------------------|
| Signals   | I/O | Pin Number | Connected with          | Description  |                                   |
| IFSEL   | I   | 1          | MPU                     | Interface format select pin  |                                   |
|   |     |            |                         | <b>IFSEL</b>   | <b>Interface Format Selection</b> |
|   |     |            |                         | 0  | Register-content interface mode   |
|   |     |            |                         | 1  | Command-Parameter interface mode  |
| In this document, the IFSEL has to be connected to GND and Register-Content interface mode is select. |     |            |                         |  |                                   |
| IM3, IM2,IM1,IM0  | I   | 4          | VSSD/<br>IOVCC          | System interface select.   |                                   |
|   |     |            |                         | <b>IM3</b> <b>IM2</b> <b>IM1</b> <b>IM0</b>  | <b>Interface</b>                  |
|   |     |            |                         | 0 0 0 0  | 8080 MCU 16-bit Parallel type I   |
|   |     |            |                         | 0 0 0 1  | 8080 MCU 8-bit Parallel type I    |
|   |     |            |                         | 0 0 1 0  | 8080 MCU 16-bit Parallel type II  |
|   |     |            |                         | 0 0 1 1  | 8080 MCU 8-bit Parallel type II   |
|   |     |            |                         | 0 1 0 ID   | 3-wire serial interface I         |
|   |     |            |                         | 0 1 1 -  | 4-wire serial interface I         |
|   |     |            |                         | 1 0 0 0  | 8080 MCU 18-bit parallel type I   |
|   |     |            |                         | 1 0 0 1  | 8080 MCU 9-bit parallel type I    |
|   |     |            |                         | 1 0 1 0  | 8080 MCU 18-bit parallel type II  |
|   |     |            |                         | 1 0 1 1  | 8080 MCU 9-bit parallel type II   |
|   |     |            |                         | 1 1 0 ID   | 3-wire serial interface II        |
|   |     |            |                         | 1 1 1 -  | 4-wire serial interface II        |
| If not used, please fix this pin to IOVCC or VSSD level.  |     |            |                         |  |                                   |
| NCS   | I   | 1          | MPU                     | Chip select signal.<br>Low: chip can be accessed;<br>High: chip cannot be accessed. Must be connected to VSSD if not in use.   |                                   |
| NWR_SCL   | I   | 1          | MPU                     | (NWR) Write enable pin I80 parallel bus system interface.<br>(SCL) server as serial data clock in serial bus system interface when IFSEL=0.<br>Fix it to IOVCC or VSSD level when not used.  |                                   |
| NRD   | I   | 1          | MPU                     | (NRD) Read enable pin I80 parallel bus system interface.<br>If not used, please fix this pin at IOVCC or GND level   |                                   |
| SDI/SDA   | I/O | 1          | MCU                     | Serial data input pin and output pin(SDA) in serial bus system interface I.<br>Serial data input pin (SDI) in serial bus system interface II.<br>The data is inputted on the rising edge of the SCL signal.<br>If not used, please let it open or connected to VSSD. |                                   |
| DNC_SCL   | I   | 1          | MPU                     | (DNC) Command / parameter or display data selection pin.<br>(SCL) server as serial data clock in serial bus system interface when IFSEL=1.<br>If not used, please fix this pin at IOVCC or GND level.  |                                   |
| VSYNC   | I   | 1          | MPU                     | Vertical synchronizing signal in RGB interface. Has to be fixed to VSSD level if it is not used.   |                                   |
| HSYNC   | I   | 1          | MPU                     | Horizontal synchronizing signal in RGB interface. Has to be fixed to VSSD level if it is not used.   |                                   |
| DE  | I   | 1          | MPU                     | A data ENABLE signal in RGB I/F mode. Has to be fixed to VSSD level if it is not used.   |                                   |
| DOTCLK  | I   | 1          | MPU                     | Data enable signal in RGB interface. Has to be fixed to VSSD level if it is not used.  |                                   |
| NRESET  | I   | 1          | MPU or<br>reset circuit | Reset pin. Setting either pin low initializes the LSI. Must be reset after power is supplied.  |                                   |
| DB17~0  | I/O | 18         | MPU                     | 18-bit bi-directional data bus.<br>The unused pins should be left open or connected to VSSD.   |                                   |

|              |   |     |                      |  |
|--------------|---|-----|----------------------|--|
| S1~S720      | O | 720 | LCD                  | Output voltages applied to the liquid crystal.   |
| G1~G320      | O | 320 | LCD                  | Gate driver output pins. These pins output VGH, VGL. (If not used, should be open)   |
| VCOM         | O | 8   | TFT common electrode | The power supply of common voltage in TFT driving. The voltage amplitude between VCOMH and VCOML is output. Connect this pin to the common electrode in TFT panel. |
| TE           | O | 1   | MPU                  | Tearing effect output.<br>If not used, please open this pin.   |
| CABC_PWM_OUT | O | 1   | Backlight Circuit    | CABC backlight control PWM signal output<br>If not used, please open this pin.   |
| BC_CTL       | O | 1   | Backlight Circuit    | LED Driver Enable Signal.<br>If not used, please open this pin.  |
| TEST3/SDO    | O | 1   | MPU                  | Serial data output pin (SDO) in serial bus system interface II.<br>If not used, please open this pin.  |

| Input/Output Part       |     |            |                   |  |
|-------------------------|-----|------------|-------------------|--|
| Signals                 | I/O | Pin Number | Connected with    | Description  |
| C11P,C11N<br>C12P, C12N | I/O | 7          | Step-up Capacitor | Connect to the step-up capacitors according to the step-up 1 factor. Leave this pin open if the internal step-up circuit is not used.                |
| C31P,C31N               | I/O | 8          | Step-up Capacitor | Connect to the step-up capacitors for step up circuit 3 operation. Leave this pin open if the internal step-up circuit is not used.                  |
| C21P,C21N<br>C22P,C22N  | I/O | 2          | Step-up Capacitor | Connect these pins to the capacitors for the step-up circuit 2. According to the step-up rate. When not using the step-up circuit2, disconnect them. |

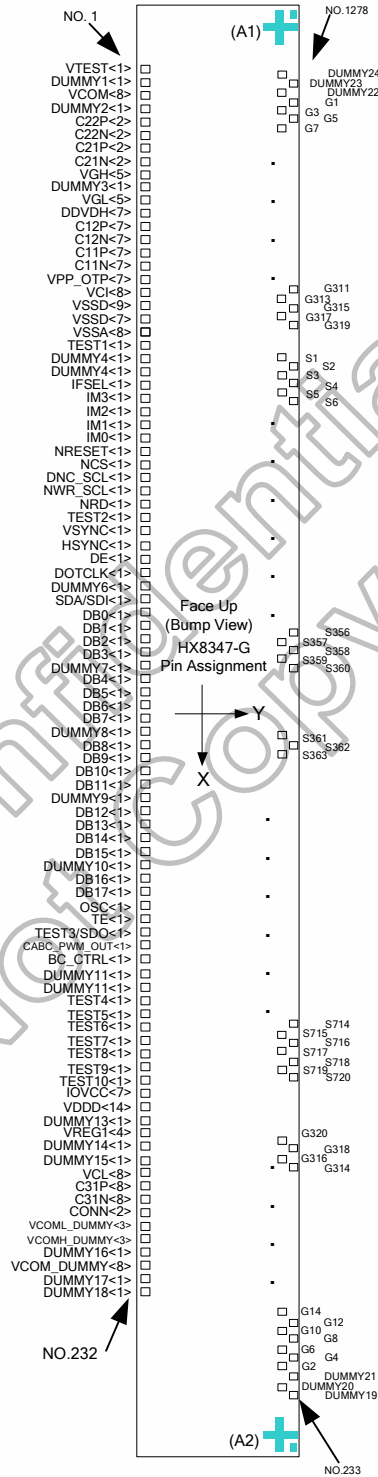
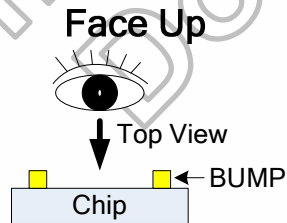
| Power Part |     |            |                       |   |
|------------|-----|------------|-----------------------|---|
| Signals    | I/O | Pin Number | Connected with        | Description   |
| IOVCC      | P   | 7          | Power Supply          | Digital IO Pad power supply   |
| VCI        | P   | 8          | Power Supply          | Analog power supply   |
| VSSD       | P   | 16         | Ground                | Digital ground  |
| VSSA       | P   | 8          | Ground                | Analog ground   |
| VDDD       | O   | 14         | Stabilizing capacitor | Output from internal logic voltage (1.4V). Connect to a stabilizing capacitor   |
| VREG1      | P   | 4          |                       | Internal generated stable power for source driver unit.   |
| VCL        | P   | 8          | Stabilizing capacitor | An output from the step-up circuit3.<br>A negative voltage for VCOML circuit, VCL=-VCI  |
| DDVDH      | P   | 7          | Stabilizing capacitor | An output from the step-up circuit1.<br>Connect to a stabilizing capacitor between VSSA and DDVDH.  |
| VGH        | P   | 5          | Stabilizing capacitor | A positive power output from the step-up circuit 2 for the gate line drive circuit.<br>The step-up rate is determined by BT3-0 bits. Connect to a stabilizing capacitor between GND and VGH.    |
| VGL        | P   | 5          | Stabilizing capacitor | A negative power output from the step-up circuit 2 for the gate line drive circuit.<br>The step-up rate is determined by BT (3-0) bits. Connect to a stabilizing capacitor between GND and VGL. |
| VPP_OTP    | -   | 7          | Power supply          | Power supply pin used in OTP program mode and operates at 6.5V ± 0.2.<br>If not in OTP program mode, please let it open or fix to GND.  |

| Test pin and others |     |            |                |   |
|---------------------|-----|------------|----------------|---|
| Signals             | I/O | Pin Number | Connected with | Description   |
| TEST2-1             | I   | 3          | GND            | Test pin input (Internal pull low). Disconnect it.  |
| TEST10-4            | O   | 8          | Open           | A test pin. Disconnect it.  |
| OSC                 | I   | 1          | Open           | A test pin. Disconnect it.  |
| VTEST               | O   | 1          | Open           | Gamma voltage of Panel test pin output. Must be left open.  |
| CONN                | -   | 2          | Open           | Dummy pads. Available for measuring the COG contact resistance. They are short-circuited within the chip. |
| VCOMH_DUMMY         | -   | 2          | Open           | Dummy pads  |
| VCOML_DUMMY         | -   | 2          | Open           | Dummy pads  |
| VCOM_DUMMY          | -   | 8          | Open/VCOM      | Dummy pads. Users can connect with VCOM.  |
| DUMMY               | -   | 24         | Open           | Dummy pads  |



## 3.3 Pin assignment

Chip Size: 15260umx720um  
 (Including Seal-ring and Scribe line)  
 Chip Thickness: 250 um (typ.)  
 Pad Location: Pad center  
 Coordinate Origin: Chip center  
 Au Bump Size:  
 1. 40 um x 56 um  
 Input Pads  
 (No. 1 ~ No. 232)  
 2. 14 um x 104 um  
 Staggered LCD output side  
 (No. 233 ~ No. 1278)



## 3.4 PAD coordinates

| No | Name   | X       | Y    | No. | Name    | X       | Y    | No. | Name         | X      | Y    | No. | Name        | X      | Y    |
|----|--------|---------|------|-----|---------|---------|------|-----|--------------|--------|------|-----|-------------|--------|------|
| 1  | VTEST  | -7292.5 | -285 | 61  | C11N    | -3692.5 | -285 | 121 | HSYNC        | -92.5  | -285 | 181 | VDDD        | 4232.5 | -285 |
| 2  | DUMMY1 | -7232.5 | -285 | 62  | C11N    | -3632.5 | -285 | 122 | DE           | -32.5  | -285 | 182 | VDDD        | 4292.5 | -285 |
| 3  | VCOM   | -7172.5 | -285 | 63  | C11N    | -3572.5 | -285 | 123 | DOTCLK       | 27.5   | -285 | 183 | DUMMY13     | 4352.5 | -285 |
| 4  | VCOM   | -7112.5 | -285 | 64  | C11N    | -3512.5 | -285 | 124 | DUMMY6       | 87.5   | -285 | 184 | VREG1       | 4412.5 | -285 |
| 5  | VCOM   | -7052.5 | -285 | 65  | C11N    | -3452.5 | -285 | 125 | SDA          | 160    | -285 | 185 | VREG1       | 4472.5 | -285 |
| 6  | VCOM   | -6992.5 | -285 | 66  | C11N    | -3392.5 | -285 | 126 | DB0          | 245    | -285 | 186 | VREG1       | 4532.5 | -285 |
| 7  | VCOM   | -6932.5 | -285 | 67  | VPP_OTP | -3332.5 | -285 | 127 | DB1          | 330    | -285 | 187 | VREG1       | 4592.5 | -285 |
| 8  | VCOM   | -6872.5 | -285 | 68  | VPP_OTP | -3272.5 | -285 | 128 | DB2          | 415    | -285 | 188 | DUMMY14     | 4652.5 | -285 |
| 9  | VCOM   | -6812.5 | -285 | 69  | VPP_OTP | -3212.5 | -285 | 129 | DB3          | 500    | -285 | 189 | DUMMY15     | 4712.5 | -285 |
| 10 | VCOM   | -6752.5 | -285 | 70  | VPP_OTP | -3152.5 | -285 | 130 | DUMMY7       | 572.5  | -285 | 190 | VCL         | 4772.5 | -285 |
| 11 | DUMMY2 | -6692.5 | -285 | 71  | VPP_OTP | -3092.5 | -285 | 131 | DB4          | 645    | -285 | 191 | VCL         | 4832.5 | -285 |
| 12 | C22P   | -6632.5 | -285 | 72  | VPP_OTP | -3032.5 | -285 | 132 | DB5          | 730    | -285 | 192 | VCL         | 4892.5 | -285 |
| 13 | C22P   | -6572.5 | -285 | 73  | VPP_OTP | -2972.5 | -285 | 133 | DB6          | 815    | -285 | 193 | VCL         | 4952.5 | -285 |
| 14 | C22N   | -6512.5 | -285 | 74  | VCI     | -2912.5 | -285 | 134 | DB7          | 900    | -285 | 194 | VCL         | 5012.5 | -285 |
| 15 | C22N   | -6452.5 | -285 | 75  | VCI     | -2852.5 | -285 | 135 | DUMMY8       | 972.5  | -285 | 195 | VCL         | 5072.5 | -285 |
| 16 | C21P   | -6392.5 | -285 | 76  | VCI     | -2792.5 | -285 | 136 | DB8          | 1045   | -285 | 196 | VCL         | 5132.5 | -285 |
| 17 | C21P   | -6332.5 | -285 | 77  | VCI     | -2732.5 | -285 | 137 | DB9          | 1130   | -285 | 197 | VCL         | 5192.5 | -285 |
| 18 | C21N   | -6272.5 | -285 | 78  | VCI     | -2672.5 | -285 | 138 | DB10         | 1215   | -285 | 198 | C31P        | 5252.5 | -285 |
| 19 | C21N   | -6212.5 | -285 | 79  | VCI     | -2612.5 | -285 | 139 | DB11         | 1300   | -285 | 199 | C31P        | 5312.5 | -285 |
| 20 | VGH    | -6152.5 | -285 | 80  | VCI     | -2552.5 | -285 | 140 | DUMMY9       | 1372.5 | -285 | 200 | C31P        | 5372.5 | -285 |
| 21 | VGH    | -6092.5 | -285 | 81  | VCI     | -2492.5 | -285 | 141 | DB12         | 1445   | -285 | 201 | C31P        | 5432.5 | -285 |
| 22 | VGH    | -6032.5 | -285 | 82  | VSSC    | -2432.5 | -285 | 142 | DB13         | 1530   | -285 | 202 | C31P        | 5492.5 | -285 |
| 23 | VGH    | -5972.5 | -285 | 83  | VSSC    | -2372.5 | -285 | 143 | DB14         | 1615   | -285 | 203 | C31P        | 5552.5 | -285 |
| 24 | VGH    | -5912.5 | -285 | 84  | VSSC    | -2312.5 | -285 | 144 | DB15         | 1700   | -285 | 204 | C31P        | 5612.5 | -285 |
| 25 | DUMMY3 | -5852.5 | -285 | 85  | VSSC    | -2252.5 | -285 | 145 | DUMMY10      | 1772.5 | -285 | 205 | C31P        | 5672.5 | -285 |
| 26 | VGL    | -5792.5 | -285 | 86  | VSSC    | -2192.5 | -285 | 146 | DB16         | 1845   | -285 | 206 | C31N        | 5732.5 | -285 |
| 27 | VGL    | -5732.5 | -285 | 87  | VSSC    | -2132.5 | -285 | 147 | DB17         | 1930   | -285 | 207 | C31N        | 5792.5 | -285 |
| 28 | VGL    | -5672.5 | -285 | 88  | VSSC    | -2072.5 | -285 | 148 | OSC          | 2002.5 | -285 | 208 | C31N        | 5852.5 | -285 |
| 29 | VGL    | -5612.5 | -285 | 89  | VSSC    | -2012.5 | -285 | 149 | TE           | 2075   | -285 | 209 | C31N        | 5912.5 | -285 |
| 30 | VGL    | -5552.5 | -285 | 90  | VSSC    | -1952.5 | -285 | 150 | TEST3/SDO    | 2160   | -285 | 210 | C31N        | 5972.5 | -285 |
| 31 | VGL    | -5492.5 | -285 | 91  | VSSD    | -1892.5 | -285 | 151 | CABC_PWM_OUT | 2245   | -285 | 211 | C31N        | 6032.5 | -285 |
| 32 | DDVDH  | -5432.5 | -285 | 92  | VSSD    | -1832.5 | -285 | 152 | BC_CTRL      | 2330   | -285 | 212 | C31N        | 6092.5 | -285 |
| 33 | DDVDH  | -5372.5 | -285 | 93  | VSSD    | -1772.5 | -285 | 153 | DUMMY11      | 2402.5 | -285 | 213 | C31N        | 6152.5 | -285 |
| 34 | DDVDH  | -5312.5 | -285 | 94  | VSSD    | -1712.5 | -285 | 154 | DUMMY11      | 2462.5 | -285 | 214 | CONN        | 6212.5 | -285 |
| 35 | DDVDH  | -5252.5 | -285 | 95  | VSSD    | -1652.5 | -285 | 155 | TEST4        | 2535   | -285 | 215 | CONN        | 6272.5 | -285 |
| 36 | DDVDH  | -5192.5 | -285 | 96  | VSSD    | -1592.5 | -285 | 156 | TEST5        | 2620   | -285 | 216 | VCOML_DUMMY | 6332.5 | -285 |
| 37 | DDVDH  | -5132.5 | -285 | 97  | VSSD    | -1532.5 | -285 | 157 | TEST6        | 2705   | -285 | 217 | VCOML_DUMMY | 6392.5 | -285 |
| 38 | DDVDH  | -5072.5 | -285 | 98  | VSSA    | -1472.5 | -285 | 158 | TEST7        | 2790   | -285 | 218 | VCOML_DUMMY | 6452.5 | -285 |
| 39 | C12P   | -5012.5 | -285 | 99  | VSSA    | -1412.5 | -285 | 159 | TEST8        | 2875   | -285 | 219 | VCOMH_DUMMY | 6512.5 | -285 |
| 40 | C12P   | -4952.5 | -285 | 100 | VSSA    | -1352.5 | -285 | 160 | TEST9        | 2960   | -285 | 220 | VCOMH_DUMMY | 6572.5 | -285 |
| 41 | C12P   | -4892.5 | -285 | 101 | VSSA    | -1292.5 | -285 | 161 | TEST10       | 3032.5 | -285 | 221 | VCOMH_DUMMY | 6632.5 | -285 |
| 42 | C12P   | -4832.5 | -285 | 102 | VSSA    | -1232.5 | -285 | 162 | IOVCC        | 3092.5 | -285 | 222 | DUMMY16     | 6692.5 | -285 |
| 43 | C12P   | -4772.5 | -285 | 103 | VSSA    | -1172.5 | -285 | 163 | IOVCC        | 3152.5 | -285 | 223 | VCOM_DUMMY  | 6752.5 | -285 |
| 44 | C12P   | -4712.5 | -285 | 104 | VSSA    | -1112.5 | -285 | 164 | IOVCC        | 3212.5 | -285 | 224 | VCOM_DUMMY  | 6812.5 | -285 |
| 45 | C12P   | -4652.5 | -285 | 105 | VSSA    | -1052.5 | -285 | 165 | IOVCC        | 3272.5 | -285 | 225 | VCOM_DUMMY  | 6872.5 | -285 |
| 46 | C12N   | -4592.5 | -285 | 106 | TEST1   | -992.5  | -285 | 166 | IOVCC        | 3332.5 | -285 | 226 | VCOM_DUMMY  | 6932.5 | -285 |
| 47 | C12N   | -4532.5 | -285 | 107 | DUMMY4  | -932.5  | -285 | 167 | IOVCC        | 3392.5 | -285 | 227 | VCOM_DUMMY  | 6992.5 | -285 |
| 48 | C12N   | -4472.5 | -285 | 108 | DUMMY4  | -872.5  | -285 | 168 | IOVCC        | 3452.5 | -285 | 228 | VCOM_DUMMY  | 7052.5 | -285 |
| 49 | C12N   | -4412.5 | -285 | 109 | IFSEL   | -812.5  | -285 | 169 | VDDD         | 3512.5 | -285 | 229 | VCOM_DUMMY  | 7112.5 | -285 |
| 50 | C12N   | -4352.5 | -285 | 110 | IM3     | -752.5  | -285 | 170 | VDDD         | 3572.5 | -285 | 230 | VCOM_DUMMY  | 7172.5 | -285 |
| 51 | C12N   | -4292.5 | -285 | 111 | IM2     | -692.5  | -285 | 171 | VDDD         | 3632.5 | -285 | 231 | DUMMY17     | 7232.5 | -285 |
| 52 | C12N   | -4232.5 | -285 | 112 | IM1     | -632.5  | -285 | 172 | VDDD         | 3692.5 | -285 | 232 | DUMMY18     | 7292.5 | -285 |
| 53 | C11P   | -4172.5 | -285 | 113 | IMO     | -572.5  | -285 | 173 | VDDD         | 3752.5 | -285 | 233 | DUMMY19     | 7399   | 261  |
| 54 | C11P   | -4112.5 | -285 | 114 | NRESET  | -512.5  | -285 | 174 | VDDD         | 3812.5 | -285 | 234 | DUMMY20     | 7385   | 126  |
| 55 | C11P   | -4052.5 | -285 | 115 | NCS     | -452.5  | -285 | 175 | VDDD         | 3872.5 | -285 | 235 | DUMMY21     | 7371   | 261  |
| 56 | C11P   | -3992.5 | -285 | 116 | DNC_SCL | -392.5  | -285 | 176 | VDDD         | 3932.5 | -285 | 236 | G2          | 7357   | 126  |
| 57 | C11P   | -3932.5 | -285 | 117 | NWR_SCL | -332.5  | -285 | 177 | VDDD         | 3992.5 | -285 | 237 | G4          | 7343   | 261  |
| 58 | C11P   | -3872.5 | -285 | 118 | NRD     | -272.5  | -285 | 178 | VDDD         | 4052.5 | -285 | 238 | G6          | 7329   | 126  |
| 59 | C11P   | -3812.5 | -285 | 119 | TEST2   | -212.5  | -285 | 179 | VDDD         | 4112.5 | -285 | 239 | G8          | 7315   | 261  |
| 60 | C11N   | -3752.5 | -285 | 120 | VSYNC   | -152.5  | -285 | 180 | VDDD         | 4172.5 | -285 | 240 | G10         | 7301   | 126  |

| No. | Name | X    | Y   | No. | Name | X    | Y   | No. | Name | X    | Y   | No. | Name | X    | Y   |
|-----|------|------|-----|-----|------|------|-----|-----|------|------|-----|-----|------|------|-----|
| 241 | G12  | 7287 | 261 | 301 | G132 | 6447 | 261 | 361 | G252 | 5607 | 261 | 421 | S695 | 4725 | 261 |
| 242 | G14  | 7273 | 126 | 302 | G134 | 6433 | 126 | 362 | G254 | 5593 | 126 | 422 | S694 | 4711 | 126 |
| 243 | G16  | 7259 | 261 | 303 | G136 | 6419 | 261 | 363 | G256 | 5579 | 261 | 423 | S693 | 4697 | 261 |
| 244 | G18  | 7245 | 126 | 304 | G138 | 6405 | 126 | 364 | G258 | 5565 | 126 | 424 | S692 | 4683 | 126 |
| 245 | G20  | 7231 | 261 | 305 | G140 | 6391 | 261 | 365 | G260 | 5551 | 261 | 425 | S691 | 4669 | 261 |
| 246 | G22  | 7217 | 126 | 306 | G142 | 6377 | 126 | 366 | G262 | 5537 | 126 | 426 | S690 | 4655 | 126 |
| 247 | G24  | 7203 | 261 | 307 | G144 | 6363 | 261 | 367 | G264 | 5523 | 261 | 427 | S689 | 4641 | 261 |
| 248 | G26  | 7189 | 126 | 308 | G146 | 6349 | 126 | 368 | G266 | 5509 | 126 | 428 | S688 | 4627 | 126 |
| 249 | G28  | 7175 | 261 | 309 | G148 | 6335 | 261 | 369 | G268 | 5495 | 261 | 429 | S687 | 4613 | 261 |
| 250 | G30  | 7161 | 126 | 310 | G150 | 6321 | 126 | 370 | G270 | 5481 | 126 | 430 | S686 | 4599 | 126 |
| 251 | G32  | 7147 | 261 | 311 | G152 | 6307 | 261 | 371 | G272 | 5467 | 261 | 431 | S685 | 4585 | 261 |
| 252 | G34  | 7133 | 126 | 312 | G154 | 6293 | 126 | 372 | G274 | 5453 | 126 | 432 | S684 | 4571 | 126 |
| 253 | G36  | 7119 | 261 | 313 | G156 | 6279 | 261 | 373 | G276 | 5439 | 261 | 433 | S683 | 4557 | 261 |
| 254 | G38  | 7105 | 126 | 314 | G158 | 6265 | 126 | 374 | G278 | 5425 | 126 | 434 | S682 | 4543 | 126 |
| 255 | G40  | 7091 | 261 | 315 | G160 | 6251 | 261 | 375 | G280 | 5411 | 261 | 435 | S681 | 4529 | 261 |
| 256 | G42  | 7077 | 126 | 316 | G162 | 6237 | 126 | 376 | G282 | 5397 | 126 | 436 | S680 | 4515 | 126 |
| 257 | G44  | 7063 | 261 | 317 | G164 | 6223 | 261 | 377 | G284 | 5383 | 261 | 437 | S679 | 4501 | 261 |
| 258 | G46  | 7049 | 126 | 318 | G166 | 6209 | 126 | 378 | G286 | 5369 | 126 | 438 | S678 | 4487 | 126 |
| 259 | G48  | 7035 | 261 | 319 | G168 | 6195 | 261 | 379 | G288 | 5355 | 261 | 439 | S677 | 4473 | 261 |
| 260 | G50  | 7021 | 126 | 320 | G170 | 6181 | 126 | 380 | G290 | 5341 | 126 | 440 | S676 | 4459 | 126 |
| 261 | G52  | 7007 | 261 | 321 | G172 | 6167 | 261 | 381 | G292 | 5327 | 261 | 441 | S675 | 4445 | 261 |
| 262 | G54  | 6993 | 126 | 322 | G174 | 6153 | 126 | 382 | G294 | 5313 | 126 | 442 | S674 | 4431 | 126 |
| 263 | G56  | 6979 | 261 | 323 | G176 | 6139 | 261 | 383 | G296 | 5299 | 261 | 443 | S673 | 4417 | 261 |
| 264 | G58  | 6965 | 126 | 324 | G178 | 6125 | 126 | 384 | G298 | 5285 | 126 | 444 | S672 | 4403 | 126 |
| 265 | G60  | 6951 | 261 | 325 | G180 | 6111 | 261 | 385 | G300 | 5271 | 261 | 445 | S671 | 4389 | 261 |
| 266 | G62  | 6937 | 126 | 326 | G182 | 6097 | 126 | 386 | G302 | 5257 | 126 | 446 | S670 | 4375 | 126 |
| 267 | G64  | 6923 | 261 | 327 | G184 | 6083 | 261 | 387 | G304 | 5243 | 261 | 447 | S669 | 4361 | 261 |
| 268 | G66  | 6909 | 126 | 328 | G186 | 6069 | 126 | 388 | G306 | 5229 | 126 | 448 | S668 | 4347 | 126 |
| 269 | G68  | 6895 | 261 | 329 | G188 | 6055 | 261 | 389 | G308 | 5215 | 261 | 449 | S667 | 4333 | 261 |
| 270 | G70  | 6881 | 126 | 330 | G190 | 6041 | 126 | 390 | G310 | 5201 | 126 | 450 | S666 | 4319 | 126 |
| 271 | G72  | 6867 | 261 | 331 | G192 | 6027 | 261 | 391 | G312 | 5187 | 261 | 451 | S665 | 4305 | 261 |
| 272 | G74  | 6853 | 126 | 332 | G194 | 6013 | 126 | 392 | G314 | 5173 | 126 | 452 | S664 | 4291 | 126 |
| 273 | G76  | 6839 | 261 | 333 | G196 | 5999 | 261 | 393 | G316 | 5159 | 261 | 453 | S663 | 4277 | 261 |
| 274 | G78  | 6825 | 126 | 334 | G198 | 5985 | 126 | 394 | G318 | 5145 | 126 | 454 | S662 | 4263 | 126 |
| 275 | G80  | 6811 | 261 | 335 | G200 | 5971 | 261 | 395 | G320 | 5131 | 261 | 455 | S661 | 4249 | 261 |
| 276 | G82  | 6797 | 126 | 336 | G202 | 5957 | 126 | 396 | G322 | 5117 | 126 | 456 | S660 | 4235 | 126 |
| 277 | G84  | 6783 | 261 | 337 | G204 | 5943 | 261 | 397 | G324 | 5103 | 261 | 457 | S659 | 4221 | 261 |
| 278 | G86  | 6769 | 126 | 338 | G206 | 5929 | 126 | 398 | G326 | 5089 | 126 | 458 | S658 | 4207 | 126 |
| 279 | G88  | 6755 | 261 | 339 | G208 | 5915 | 261 | 399 | G328 | 5075 | 261 | 459 | S657 | 4193 | 261 |
| 280 | G90  | 6741 | 126 | 340 | G210 | 5901 | 126 | 400 | G330 | 5061 | 126 | 460 | S656 | 4179 | 126 |
| 281 | G92  | 6727 | 261 | 341 | G212 | 5887 | 261 | 401 | G332 | 5047 | 261 | 461 | S655 | 4165 | 261 |
| 282 | G94  | 6713 | 126 | 342 | G214 | 5873 | 126 | 402 | G334 | 5033 | 126 | 462 | S654 | 4151 | 126 |
| 283 | G96  | 6699 | 261 | 343 | G216 | 5859 | 261 | 403 | G336 | 5019 | 261 | 463 | S653 | 4137 | 261 |
| 284 | G98  | 6685 | 126 | 344 | G218 | 5845 | 126 | 404 | G338 | 5005 | 126 | 464 | S652 | 4123 | 126 |
| 285 | G100 | 6671 | 261 | 345 | G220 | 5831 | 261 | 405 | G340 | 4991 | 126 | 465 | S651 | 4109 | 261 |
| 286 | G102 | 6657 | 126 | 346 | G222 | 5817 | 126 | 406 | G342 | 4977 | 261 | 466 | S650 | 4095 | 126 |
| 287 | G104 | 6643 | 261 | 347 | G224 | 5803 | 261 | 407 | G344 | 4963 | 126 | 467 | S649 | 4081 | 261 |
| 288 | G106 | 6629 | 126 | 348 | G226 | 5789 | 126 | 408 | G346 | 4949 | 261 | 468 | S648 | 4067 | 126 |
| 289 | G108 | 6615 | 261 | 349 | G228 | 5775 | 261 | 409 | G348 | 4935 | 126 | 469 | S647 | 4053 | 261 |
| 290 | G110 | 6601 | 126 | 350 | G230 | 5761 | 126 | 410 | G350 | 4921 | 261 | 470 | S646 | 4039 | 126 |
| 291 | G112 | 6587 | 261 | 351 | G232 | 5747 | 261 | 411 | G352 | 4907 | 126 | 471 | S645 | 4025 | 261 |
| 292 | G114 | 6573 | 126 | 352 | G234 | 5733 | 126 | 412 | G354 | 4893 | 126 | 472 | S644 | 4011 | 126 |
| 293 | G116 | 6559 | 261 | 353 | G236 | 5719 | 261 | 413 | G356 | 4879 | 126 | 473 | S643 | 3997 | 261 |
| 294 | G118 | 6545 | 126 | 354 | G238 | 5705 | 126 | 414 | G358 | 4865 | 261 | 474 | S642 | 3983 | 126 |
| 295 | G120 | 6531 | 261 | 355 | G240 | 5691 | 261 | 415 | G360 | 4851 | 126 | 475 | S641 | 3969 | 261 |
| 296 | G122 | 6517 | 126 | 356 | G242 | 5677 | 126 | 416 | G362 | 4837 | 261 | 476 | S640 | 3955 | 126 |
| 297 | G124 | 6503 | 261 | 357 | G244 | 5663 | 261 | 417 | G364 | 4823 | 126 | 477 | S639 | 3941 | 261 |
| 298 | G126 | 6489 | 126 | 358 | G246 | 5649 | 126 | 418 | G366 | 4809 | 261 | 478 | S638 | 3927 | 126 |
| 299 | G128 | 6475 | 261 | 359 | G248 | 5635 | 261 | 419 | G368 | 4795 | 126 | 479 | S637 | 3913 | 261 |
| 300 | G130 | 6461 | 126 | 360 | G250 | 5621 | 126 | 420 | G370 | 4781 | 261 | 480 | S636 | 3899 | 126 |

| No. | Name | X    | Y   | No. | Name | X    | Y   | No. | Name | X    | Y   | No. | Name | X    | Y   |
|-----|------|------|-----|-----|------|------|-----|-----|------|------|-----|-----|------|------|-----|
| 481 | S635 | 3885 | 261 | 541 | S575 | 3045 | 261 | 601 | S515 | 2205 | 261 | 661 | S455 | 1365 | 261 |
| 482 | S634 | 3871 | 126 | 542 | S574 | 3031 | 126 | 602 | S514 | 2191 | 126 | 662 | S454 | 1351 | 126 |
| 483 | S633 | 3857 | 261 | 543 | S573 | 3017 | 261 | 603 | S513 | 2177 | 261 | 663 | S453 | 1337 | 261 |
| 484 | S632 | 3843 | 126 | 544 | S572 | 3003 | 126 | 604 | S512 | 2163 | 126 | 664 | S452 | 1323 | 126 |
| 485 | S631 | 3829 | 261 | 545 | S571 | 2989 | 261 | 605 | S511 | 2149 | 261 | 665 | S451 | 1309 | 261 |
| 486 | S630 | 3815 | 126 | 546 | S570 | 2975 | 126 | 606 | S510 | 2135 | 126 | 666 | S450 | 1295 | 126 |
| 487 | S629 | 3801 | 261 | 547 | S569 | 2961 | 261 | 607 | S509 | 2121 | 261 | 667 | S449 | 1281 | 261 |
| 488 | S628 | 3787 | 126 | 548 | S568 | 2947 | 126 | 608 | S508 | 2107 | 126 | 668 | S448 | 1267 | 126 |
| 489 | S627 | 3773 | 261 | 549 | S567 | 2933 | 261 | 609 | S507 | 2093 | 261 | 669 | S447 | 1253 | 261 |
| 490 | S626 | 3759 | 126 | 550 | S566 | 2919 | 126 | 610 | S506 | 2079 | 126 | 670 | S446 | 1239 | 126 |
| 491 | S625 | 3745 | 261 | 551 | S565 | 2905 | 261 | 611 | S505 | 2065 | 261 | 671 | S445 | 1225 | 261 |
| 492 | S624 | 3731 | 126 | 552 | S564 | 2891 | 126 | 612 | S504 | 2051 | 126 | 672 | S444 | 1211 | 126 |
| 493 | S623 | 3717 | 261 | 553 | S563 | 2877 | 261 | 613 | S503 | 2037 | 261 | 673 | S443 | 1197 | 261 |
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| 496 | S620 | 3675 | 126 | 556 | S560 | 2835 | 126 | 616 | S500 | 1995 | 126 | 676 | S440 | 1155 | 126 |
| 497 | S619 | 3661 | 261 | 557 | S559 | 2821 | 261 | 617 | S499 | 1981 | 261 | 677 | S439 | 1141 | 261 |
| 498 | S618 | 3647 | 126 | 558 | S558 | 2807 | 126 | 618 | S498 | 1967 | 126 | 678 | S438 | 1127 | 126 |
| 499 | S617 | 3633 | 261 | 559 | S557 | 2793 | 261 | 619 | S497 | 1953 | 261 | 679 | S437 | 1113 | 261 |
| 500 | S616 | 3619 | 126 | 560 | S556 | 2779 | 126 | 620 | S496 | 1939 | 126 | 680 | S436 | 1099 | 126 |
| 501 | S615 | 3605 | 261 | 561 | S555 | 2765 | 261 | 621 | S495 | 1925 | 261 | 681 | S435 | 1085 | 261 |
| 502 | S614 | 3591 | 126 | 562 | S554 | 2751 | 126 | 622 | S494 | 1911 | 126 | 682 | S434 | 1071 | 126 |
| 503 | S613 | 3577 | 261 | 563 | S553 | 2737 | 261 | 623 | S493 | 1897 | 261 | 683 | S433 | 1057 | 261 |
| 504 | S612 | 3563 | 126 | 564 | S552 | 2723 | 126 | 624 | S492 | 1883 | 126 | 684 | S432 | 1043 | 126 |
| 505 | S611 | 3549 | 261 | 565 | S551 | 2709 | 261 | 625 | S491 | 1869 | 261 | 685 | S431 | 1029 | 261 |
| 506 | S610 | 3535 | 126 | 566 | S550 | 2695 | 126 | 626 | S490 | 1855 | 126 | 686 | S430 | 1015 | 126 |
| 507 | S609 | 3521 | 261 | 567 | S549 | 2681 | 261 | 627 | S489 | 1841 | 261 | 687 | S429 | 1001 | 261 |
| 508 | S608 | 3507 | 126 | 568 | S548 | 2667 | 126 | 628 | S488 | 1827 | 126 | 688 | S428 | 987  | 126 |
| 509 | S607 | 3493 | 261 | 569 | S547 | 2653 | 261 | 629 | S487 | 1813 | 261 | 689 | S427 | 973  | 261 |
| 510 | S606 | 3479 | 126 | 570 | S546 | 2639 | 126 | 630 | S486 | 1799 | 126 | 690 | S426 | 959  | 126 |
| 511 | S605 | 3465 | 261 | 571 | S545 | 2625 | 261 | 631 | S485 | 1785 | 261 | 691 | S425 | 945  | 261 |
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| 513 | S603 | 3437 | 261 | 573 | S543 | 2597 | 261 | 633 | S483 | 1757 | 261 | 693 | S423 | 917  | 261 |
| 514 | S602 | 3423 | 126 | 574 | S542 | 2583 | 126 | 634 | S482 | 1743 | 126 | 694 | S422 | 903  | 126 |
| 515 | S601 | 3409 | 261 | 575 | S541 | 2569 | 261 | 635 | S481 | 1729 | 261 | 695 | S421 | 889  | 261 |
| 516 | S600 | 3395 | 126 | 576 | S540 | 2555 | 126 | 636 | S480 | 1715 | 126 | 696 | S420 | 875  | 126 |
| 517 | S599 | 3381 | 261 | 577 | S539 | 2541 | 261 | 637 | S479 | 1701 | 261 | 697 | S419 | 861  | 261 |
| 518 | S598 | 3367 | 126 | 578 | S538 | 2527 | 126 | 638 | S478 | 1687 | 126 | 698 | S418 | 847  | 126 |
| 519 | S597 | 3353 | 261 | 579 | S537 | 2513 | 261 | 639 | S477 | 1673 | 261 | 699 | S417 | 833  | 261 |
| 520 | S596 | 3339 | 126 | 580 | S536 | 2499 | 126 | 640 | S476 | 1659 | 126 | 700 | S416 | 819  | 126 |
| 521 | S595 | 3325 | 261 | 581 | S535 | 2485 | 261 | 641 | S475 | 1645 | 261 | 701 | S415 | 805  | 261 |
| 522 | S594 | 3311 | 126 | 582 | S534 | 2471 | 126 | 642 | S474 | 1631 | 126 | 702 | S414 | 791  | 126 |
| 523 | S593 | 3297 | 261 | 583 | S533 | 2457 | 261 | 643 | S473 | 1617 | 261 | 703 | S413 | 777  | 261 |
| 524 | S592 | 3283 | 126 | 584 | S532 | 2443 | 126 | 644 | S472 | 1603 | 126 | 704 | S412 | 763  | 126 |
| 525 | S591 | 3269 | 261 | 585 | S531 | 2429 | 261 | 645 | S471 | 1589 | 261 | 705 | S411 | 749  | 261 |
| 526 | S590 | 3255 | 126 | 586 | S530 | 2415 | 126 | 646 | S470 | 1575 | 126 | 706 | S410 | 735  | 126 |
| 527 | S589 | 3241 | 261 | 587 | S529 | 2401 | 261 | 647 | S469 | 1561 | 261 | 707 | S409 | 721  | 261 |
| 528 | S588 | 3227 | 126 | 588 | S528 | 2387 | 126 | 648 | S468 | 1547 | 126 | 708 | S408 | 707  | 126 |
| 529 | S587 | 3213 | 261 | 589 | S527 | 2373 | 261 | 649 | S467 | 1533 | 261 | 709 | S407 | 693  | 261 |
| 530 | S586 | 3199 | 126 | 590 | S526 | 2359 | 126 | 650 | S466 | 1519 | 126 | 710 | S406 | 679  | 126 |
| 531 | S585 | 3185 | 261 | 591 | S525 | 2345 | 261 | 651 | S465 | 1505 | 261 | 711 | S405 | 665  | 261 |
| 532 | S584 | 3171 | 126 | 592 | S524 | 2331 | 126 | 652 | S464 | 1491 | 126 | 712 | S404 | 651  | 126 |
| 533 | S583 | 3157 | 261 | 593 | S523 | 2317 | 261 | 653 | S463 | 1477 | 261 | 713 | S403 | 637  | 261 |
| 534 | S582 | 3143 | 126 | 594 | S522 | 2303 | 126 | 654 | S462 | 1463 | 126 | 714 | S402 | 623  | 126 |
| 535 | S581 | 3129 | 261 | 595 | S521 | 2289 | 261 | 655 | S461 | 1449 | 261 | 715 | S401 | 609  | 261 |
| 536 | S580 | 3115 | 126 | 596 | S520 | 2275 | 126 | 656 | S460 | 1435 | 126 | 716 | S400 | 595  | 126 |
| 537 | S579 | 3101 | 261 | 597 | S519 | 2261 | 261 | 657 | S459 | 1421 | 261 | 717 | S399 | 581  | 261 |
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| 539 | S577 | 3073 | 261 | 599 | S517 | 2233 | 261 | 659 | S457 | 1393 | 261 | 719 | S397 | 553  | 261 |
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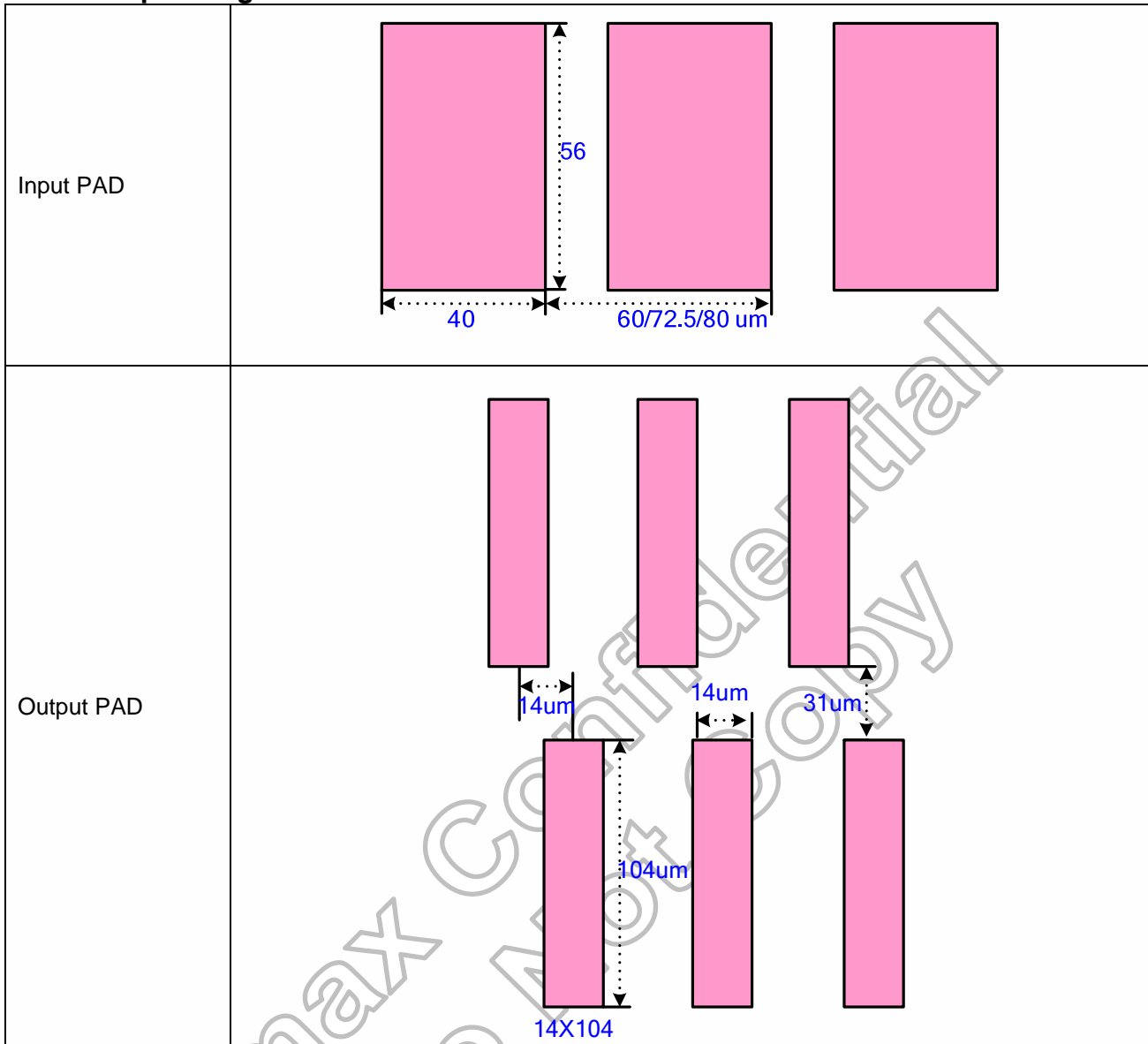
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| 722 | S394 | 511  | 126 | 782 | S334 | -413  | 126 | 842 | S274 | -1253 | 126 | 902 | S214 | -2093 | 126 |
| 723 | S393 | 497  | 261 | 783 | S333 | -427  | 261 | 843 | S273 | -1267 | 261 | 903 | S213 | -2107 | 261 |
| 724 | S392 | 483  | 126 | 784 | S332 | -441  | 126 | 844 | S272 | -1281 | 126 | 904 | S212 | -2121 | 126 |
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| 729 | S387 | 413  | 261 | 789 | S327 | -511  | 261 | 849 | S267 | -1351 | 261 | 909 | S207 | -2191 | 261 |
| 730 | S386 | 399  | 126 | 790 | S326 | -525  | 126 | 850 | S266 | -1365 | 126 | 910 | S206 | -2205 | 126 |
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| 733 | S383 | 357  | 261 | 793 | S323 | -567  | 261 | 853 | S263 | -1407 | 261 | 913 | S203 | -2247 | 261 |
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| 740 | S376 | 259  | 126 | 800 | S316 | -665  | 126 | 860 | S256 | -1505 | 126 | 920 | S196 | -2345 | 126 |
| 741 | S375 | 245  | 261 | 801 | S315 | -679  | 261 | 861 | S255 | -1519 | 261 | 921 | S195 | -2359 | 261 |
| 742 | S374 | 231  | 126 | 802 | S314 | -693  | 126 | 862 | S254 | -1533 | 126 | 922 | S194 | -2373 | 126 |
| 743 | S373 | 217  | 261 | 803 | S313 | -707  | 261 | 863 | S253 | -1547 | 261 | 923 | S193 | -2387 | 261 |
| 744 | S372 | 203  | 126 | 804 | S312 | -721  | 126 | 864 | S252 | -1561 | 126 | 924 | S192 | -2401 | 126 |
| 745 | S371 | 189  | 261 | 805 | S311 | -735  | 261 | 865 | S251 | -1575 | 261 | 925 | S191 | -2415 | 261 |
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| 747 | S369 | 161  | 261 | 807 | S309 | -763  | 261 | 867 | S249 | -1603 | 261 | 927 | S189 | -2443 | 261 |
| 748 | S368 | 147  | 126 | 808 | S308 | -777  | 126 | 868 | S248 | -1617 | 126 | 928 | S188 | -2457 | 126 |
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| 1216 | G119 | -6531 | 126 | 1276                  | DUMMY22 | -7371 | 126 |
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| 1240 | G71  | -6867 | 126 |                       |         |       |     |
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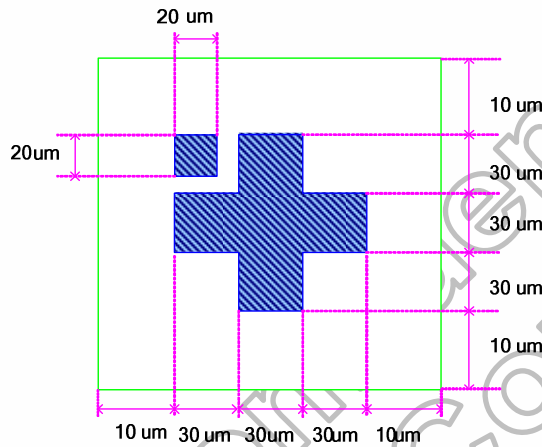
### 3.5 Bump arrangement



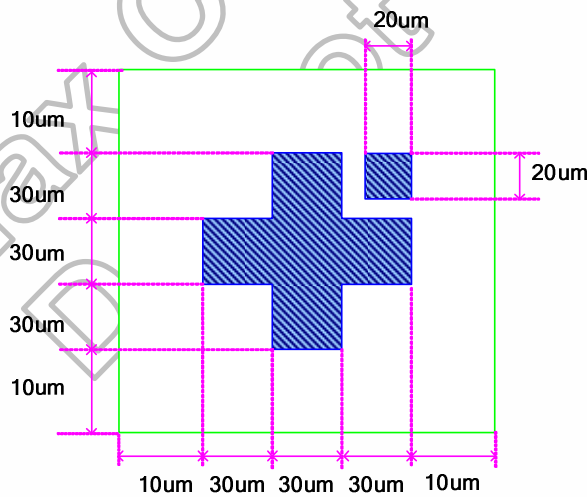
### 3.6 Alignment mark



A\_MARK (A1)



A\_MARK (A2)



## 4. Interface

The HX8347-G supports two-type interface group: Command-Parameter interface group, Register-Content interface group.

This manual description focuses on Register-Content interface group. About the Command-Parameter interface mode, please refer to the HX8347-G (N) datasheet for detail.

In Register-Content interface group (IFSEL = 'L'), the HX8347-G has a system interface circuit for register command/GRAM data transferring, and a RGB interface circuit for display data transferring during animated display. The system interface circuit uses data bus pins (DB17-0). Since the data bus pins (DB17-0) can be used as input in RGB interface circuit, the HX8347-G shows animated display with less wiring.

System interface can be used to access internal command and internal 18-bit/pixel GRAM. The RGB interface is only used to access display data. Please make sure that in RGB interface mode, the input display data is not written to GRAM and is displayed directly.

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### 4.1 System interface circuit

The system interface circuit in HX8347-G supports, 18-/16-/9-/8-bit bus width parallel bus system interface for I80 series CPU, and 4-/3-wire serial bus system interface for serial data input. When NCS = "L", the parallel and serial bus system interface of the HX8347-G become active and data transfer through the interface circuit is available. The DNC\_SCL pin specifies whether the system interface circuit access is to the register command or to the display data RAM. The input bus format of system interface circuit is selected by external pins setting. For selecting the input bus format, please refer to Table 4.1.

| IM3           | IM2 | IM1 | IM0 | Interface                        | DNC_SCL | NWR_SCL | Data Bus use     |                            |
|---------------|-----|-----|-----|----------------------------------|---------|---------|------------------|----------------------------|
|               |     |     |     |                                  |         |         | Register/Content | GRAM                       |
| 0             | 0   | 0   | 0   | 8080 MCU 16-bit parallel type I  | DNC     | NWR     | D7-D0            | D15-D0: 16-bit data        |
| 0             | 0   | 0   | 1   | 8080 MCU 8-bit parallel type I   | DNC     | NWR     | D7-D0            | D7-D0: 8-bit data          |
| 0             | 0   | 1   | 0   | 8080 MCU 16-bit parallel type II | DNC     | NWR     | D8-D1            | D17-10, D8-D1: 16-bit data |
| 0             | 0   | 1   | 1   | 8080 MCU 8-bit parallel type II  | DNC     | NWR     | D17-D10          | D17-D10: 8-bit data        |
| 0             | 1   | 0   | ID  | 3-wire serial interface          | -       | SCL     |                  | SDA                        |
| 0             | 1   | 1   | -   | 4-wire serial interface          | DNC     | SCL     |                  | SDA                        |
| 1             | 0   | 0   | 0   | 8080 MCU 18-bit parallel type I  | DNC     | NWR     | D7-D0            | D17-D0: 18-bit data        |
| 1             | 0   | 0   | 1   | 8080 MCU 9-bit parallel type I   | DNC     | NWR     | D7-D0            | D8-D0: 9-bit data          |
| 1             | 0   | 1   | 0   | 8080 MCU 18-bit parallel type II | DNC     | NWR     | D8-D1            | D17-D0: 18-bit data        |
| 1             | 0   | 1   | 1   | 8080 MCU 9-bit parallel type II  | DNC     | NWR     | D17-D10          | D17-D9: 9-bit data         |
| 1             | 1   | 0   | ID  | 3-wire serial interface II       | -       | SCL     |                  | SDI/SDO                    |
| 1             | 1   | 1   | -   | 4-wire serial interface II       | DNC     | SCL     |                  | SDI/SDO                    |
| Other Setting |     |     |     | Setting Invalid                  |         |         |                  |                            |

**Table 4.1: Input bus format selection of system interface circuit**

It has an Index Register (IR) in HX8347-G to store index data of internal control register and GRAM. Therefore, the IR can be written with the index pointer of the control register through data bus by setting DNC\_SCL=0. Then the command or GRAM data can be written to register at which that index pointer pointed by setting DNC\_SCL=1.

Furthermore, there are two 18-bit bus control registers used to temporarily store the data written to or read from the GRAM. When the data is written into the GRAM from the MPU, it is first written into the write-data latch and then automatically written into the GRAM by internal operation. Data is read through the read-data latch when reading from the GRAM. Therefore, the first read data operation is invalid and the following read data operations are valid.

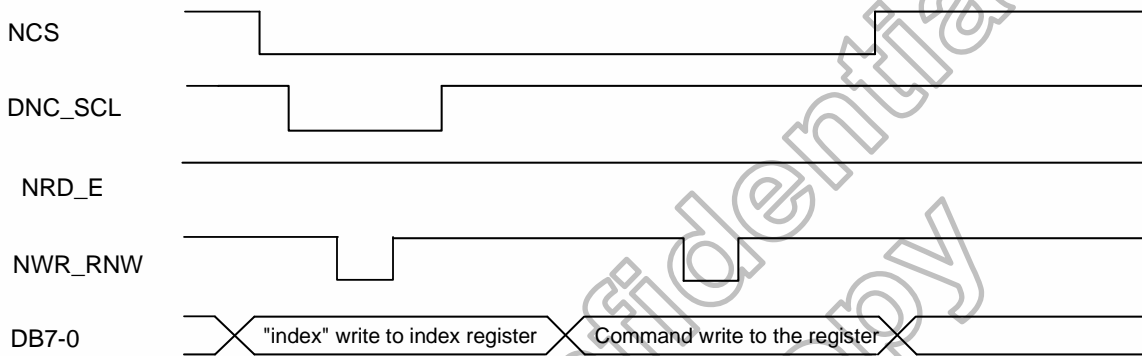
### 4.1.1 Parallel bus system interface

The input / output data from data pins (DB17-0) and signal operation of the I80 series parallel bus interface are listed in Table 4.2.

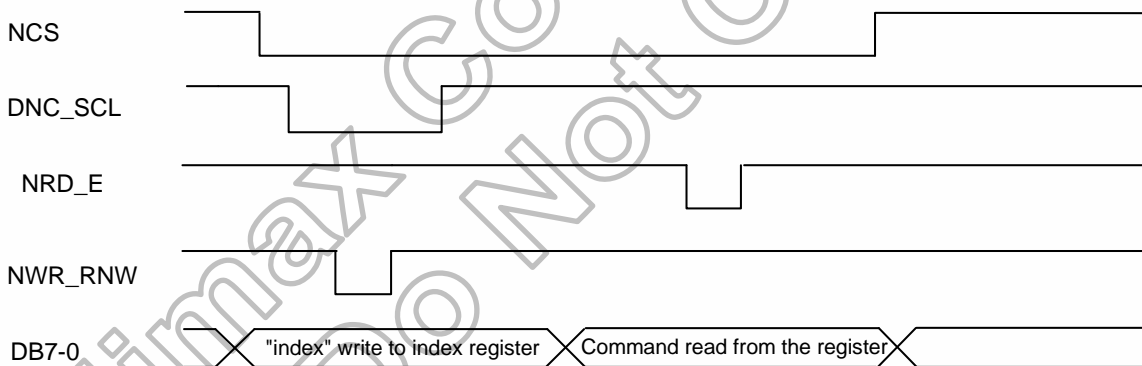
| Operations                                     | NWR_SCL | NRD | DNC_SCL |
|--|---------|-----|---------|
| Writes Indexes into IR                         | 0       | 1   | 0       |
| Reads internal status                          | 1       | 0   | 0       |
| Writes command into register or data into GRAM | 0       | 1   | 1       |
| Reads command from register or data from GRAM  | 1       | 0   | 1       |

**Table 4.2: Data pin function for I80 series CPU**

#### Write to the register

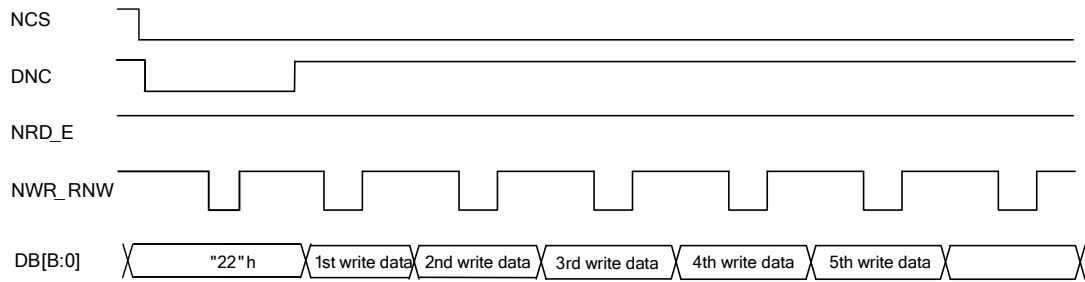


#### Read the register

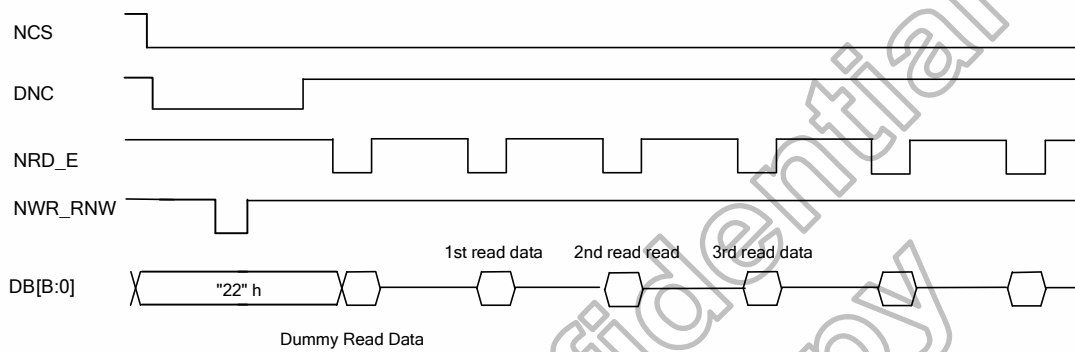


**Figure 4.1: Register read/write timing in parallel bus system interface (for I80 series MPU)**

**Write to the graphic RAM**



**Read the graphic RAM**



**Figure 4.2: GRAM read/write timing in parallel bus system interface (for l80 series MPU)**

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**4.1.2 MCU data color coding**

MCU Data Color Coding for RAM data Write

- Parallel 8-Bit Bus Interface type I (IM3,IM2,IM1,IM0="0001")

**Table 4.3: 8-bit parallel interface type I GRAM write table**

- Parallel 16-Bit Bus Interface type I (IM3,IM2,IM1,IM0="0000")

| Register Command | DB17 | DB16 | DB15 | DB14 | DB13 | DB12 | DB11 | DB10 | DB9 | DB8 | DB7 | DB6 | DB5 | DB4 | DB3 | DB2 | DB1 | DB0 | Command                          |    |    |          |
|------------------|------|------|------|------|------|------|------|------|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|----------------------------------|----|----|----------|
| 17H              | x    | x    | x    | x    | x    | x    | x    | x    | x   | x   | 0   | 0   | 1   | 0   | 0   | 0   | 1   | 0   | 22H                              |    |    |          |
| 03h              |      |      |      |      |      |      | R3   | R2   | R1  | R0  | G3  | G2  | G1  | G0  | B3  | B2  | B1  | B0  | Color                            |    |    |          |
| 05h              |      |      |      |      |      |      | R3   | R2   | R1  | R0  | G5  | G4  | G3  | G2  | G1  | G0  | B5  | B4  | B3                               | B2 | B1 | 4K-Color |
| 06h              | x    | x    | R4   | R3   | R2   | R1   | R0   | G5   | G4  | G3  | G2  | G1  | G0  | B5  | B4  | B3  | B2  | B1  | 65K-Color                        |    |    |          |
| 06h              | x    | x    | R5   | R4   | R3   | R2   | R1   | R0   | x   | x   | G5  | G4  | G3  | G2  | G1  | G0  | x   | x   | 262K-Color<br>(2-pixels/ 3bytes) |    |    |          |
|                  | x    | x    | B5   | B4   | B3   | B2   | B1   | B0   | x   | x   | R5  | R4  | R3  | R2  | R1  | R0  | x   | x   |                                  |    |    |          |
| 07h              | x    | x    | G5   | G4   | G3   | G2   | G1   | G0   | x   | x   | B5  | B4  | B3  | B2  | B1  | B0  | x   | x   | 262K-Color (16+2)                |    |    |          |
|                  | x    | x    | R5   | R4   | R3   | R2   | R1   | R0   | G5  | G4  | G3  | G2  | G1  | G0  | B5  | B4  | B3  | B2  |                                  |    |    |          |

**Table 4.4: 16-bit parallel interface type I GRAM write table**

- Parallel 9-Bit Bus Interface type I (IM3,IM2,IM1,IM0="1001")

| Register Command | DB17 | DB16 | DB15 | DB14 | DB13 | DB12 | DB11 | DB10 | DB9 | DB8 | DB7 | DB6 | DB5 | DB4 | DB3 | DB2 | DB1 | DB0 | Register                         |
|------------------|------|------|------|------|------|------|------|------|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|----------------------------------|
| 17H              | x    | x    | x    | x    | x    | x    | x    | x    | x   | x   | 0   | 0   | 1   | 0   | 0   | 0   | 1   | 0   | 22H                              |
| 06h              |      |      |      |      |      |      |      |      |     | R5  | R4  | R3  | R2  | R1  | R0  | G5  | G4  | G3  | Color                            |
| 06h              | x    | x    | x    | x    | x    | x    | x    | x    | x   | G2  | G1  | G0  | B5  | B4  | B3  | B2  | B1  | B0  | 262K-Color<br>(1-pixels/ 2bytes) |
|                  | x    | x    | x    | x    | x    | x    | x    | x    | x   | R5  | R4  | R3  | R2  | R1  | R0  | G5  | G4  | G3  |                                  |

**Table 4.5: 9-bit parallel interface type I GRAM write table**

- Parallel 18-Bit Bus Interface type I (IM3,IM2,IM1,IM0="1000")

| Register Command | DB17 | DB16 | DB15 | DB14 | DB13 | DB12 | DB11 | DB10 | DB9 | DB8 | DB7 | DB6 | DB5 | DB4 | DB3 | DB2 | DB1 | DB0 | Register   |
|------------------|------|------|------|------|------|------|------|------|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|------------|
| 17H              | x    | x    | x    | x    | x    | x    | x    | x    | x   | x   | 0   | 0   | 1   | 0   | 0   | 0   | 1   | 0   | 22H        |
| 06h              |      |      |      |      |      |      |      |      |     | R5  | R4  | R3  | R2  | R1  | R0  | G5  | G4  | G3  | Color      |
| 06h              | R5   | R4   | R3   | R2   | R1   | R0   | G5   | G4   | G3  | G2  | G1  | G0  | B5  | B4  | B3  | B2  | B1  | B0  | 262K-Color |

**Table 4.6: 18-bit parallel interface type I GRAM write table**

- Parallel 8-Bit Bus Interface typeII (IM3,IM2,IM1,IM0="0011")

| Register Command | DB17 | DB16 | DB15 | DB14 | DB13 | DB12 | DB11 | DB10 | DB9 | DB8 | DB7 | DB6 | DB5 | DB4 | DB3 | DB2 | DB1 | DB0 | Command                         |
|------------------|------|------|------|------|------|------|------|------|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|---------------------------------|
|                  | 0    | 0    | 1    | 0    | 0    | 0    | 1    | 0    | x   | x   | x   | x   | x   | x   | x   | x   | x   | x   | <b>22H</b>                      |
| <b>17H</b>       | DB17 | DB16 | DB15 | DB14 | DB13 | DB12 | DB11 | DB10 | DB9 | DB8 | DB7 | DB6 | DB5 | DB4 | DB3 | DB2 | DB1 | DB0 | Color                           |
| 03h              | R3   | R2   | R1   | R0   | G3   | G2   | G1   | G0   | x   | x   | x   | x   | x   | x   | x   | x   | x   | x   | 4K-Color<br>(2-pixels/ 3-bytes) |
|                  | B3   | B2   | B1   | B0   | R3   | R2   | R1   | R0   | x   | x   | x   | x   | x   | x   | x   | x   | x   | x   |                                 |
| 05h              | R4   | R3   | R2   | R1   | R0   | G5   | G4   | G3   | x   | x   | x   | x   | x   | x   | x   | x   | x   | x   | 65K-Color<br>(1-pixel/ 2-bytes) |
|                  | G2   | G1   | G0   | B4   | B3   | B2   | B1   | B0   | x   | x   | x   | x   | x   | x   | x   | x   | x   | x   |                                 |
| 06h              | R5   | R4   | R3   | R2   | R1   | R0   | x    | x    | x   | x   | x   | x   | x   | x   | x   | x   | x   | x   | 262K-Color<br>(1-pixel/ 3bytes) |
|                  | G5   | G4   | G3   | G2   | G1   | G0   | x    | x    | x   | x   | x   | x   | x   | x   | x   | x   | x   | x   |                                 |
|                  | B5   | B4   | B3   | B2   | B1   | B0   | x    | x    | x   | x   | x   | x   | x   | x   | x   | x   | x   | x   |                                 |

Table 4.7: 8-bit parallel interface type II GRAM write table

- Parallel 16-Bit Bus Interface typeII (IM3,IM2,IM1,IM0="0010")

| Register Command | DB17 | DB16 | DB15 | DB14 | DB13 | DB12 | DB11 | DB10 | DB9 | DB8 | DB7 | DB6 | DB5 | DB4 | DB3 | DB2 | DB1 | DB0 | Command                          |
|------------------|------|------|------|------|------|------|------|------|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|----------------------------------|
|                  |      |      |      |      |      |      |      |      | x   | 0   | 0   | 1   | 0   | 0   | 0   | 1   | 0   | x   | <b>22H</b>                       |
| <b>17H</b>       | DB17 | DB16 | DB15 | DB14 | DB13 | DB12 | DB11 | DB10 | DB9 | DB8 | DB7 | DB6 | DB5 | DB4 | DB3 | DB2 | DB1 | DB0 | Color                            |
| 03h              | x    | x    | x    | x    | R3   | R2   | R1   | R0   | x   | G3  | G2  | G1  | G0  | B3  | B2  | B1  | B0  | x   | 4K-Color                         |
| 05h              | R4   | R3   | R2   | R1   | R0   | G5   | G4   | G3   | x   | G2  | G1  | G0  | B4  | B3  | B2  | B1  | B0  | x   | 65K-Color                        |
| 06h              | R5   | R4   | R3   | R2   | R1   | R0   | x    | x    | x   | G5  | G4  | G3  | G2  | G1  | G0  | x   | x   | x   | 262K-Color<br>(2-pixels/ 3bytes) |
|                  | B5   | B4   | B3   | B2   | B1   | B0   | x    | x    | x   | R5  | R4  | R3  | R2  | R1  | R0  | x   | x   | x   |                                  |
| 07h              | G5   | G4   | G3   | G2   | G1   | G0   | x    | x    | x   | B5  | B4  | B3  | B2  | B1  | B0  | x   | x   | x   | 262K-Color (16+2)                |
|                  | R5   | R4   | R3   | R2   | R1   | R0   | G5   | G4   | x   | G3  | G2  | G1  | G0  | B5  | B4  | B3  | B2  | x   |                                  |
|                  | B1   | B0   | x    | x    | x    | x    | x    | x    | x   | x   | x   | x   | x   |     |     | x   | x   | x   |                                  |

Table 4.8: 16-bit parallel interface type II GRAM write set table

- Parallel 9-Bit Bus Interface typeII (IM3,IM2,IM1,IM0="1011")

| Register Command | D17 | D16 | D15 | D14 | D13 | D12 | D11 | D10 | D9 | D8 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | Register                        |
|------------------|-----|-----|-----|-----|-----|-----|-----|-----|----|----|----|----|----|----|----|----|----|----|---------------------------------|
|                  | 0   | 0   | 1   | 0   | 0   | 0   | 1   | 0   | x  | x  | x  | x  | x  | x  | x  | x  | x  | x  | <b>22H</b>                      |
| <b>17H</b>       | D8  | D7  | D6  | D5  | D4  | D3  | D2  | D1  | D0 | D8 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | Color                           |
| 06h              | R5  | R4  | R3  | R2  | R1  | R0  | G5  | G4  | G3 | x  | x  | x  | x  | x  | x  | x  | x  | x  | 262K-Color<br>(1-pixel/ 2bytes) |
|                  | G2  | G1  | G0  | B5  | B4  | B3  | B2  | B1  | B0 | x  | x  | x  | x  | x  | x  | x  | x  | x  |                                 |

Table 4.9: 9-bit parallel interface set type II GRAM write table

- Parallel 18-Bit Bus Interface typeII (IM3,IM2,IM1,IM0="1010")

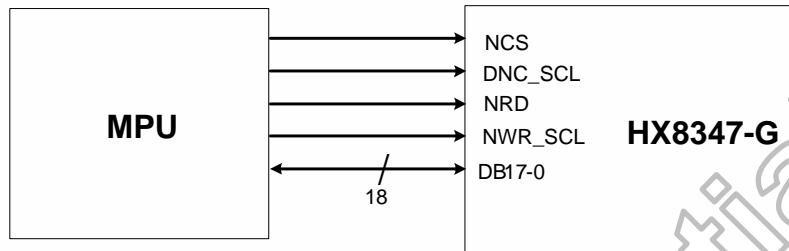
| Register Command | DB17 | DB16 | DB15 | DB14 | DB13 | DB12 | DB11 | DB10 | DB9 | DB8 | DB7 | DB6 | DB5 | DB4 | DB3 | DB2 | DB1 | DB0 | Register   |
|------------------|------|------|------|------|------|------|------|------|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|------------|
|                  | x    | x    | x    | x    | x    | x    | x    | x    | x   | 0   | 0   | 1   | 0   | 0   | 0   | 1   | 0   | x   | <b>22H</b> |
| <b>17H</b>       | DB17 | DB16 | DB15 | DB14 | DB13 | DB12 | DB11 | DB10 | DB9 | DB8 | DB7 | DB6 | DB5 | DB4 | DB3 | DB2 | DB1 | DB0 | Color      |
| 06h              | R5   | R4   | R3   | R2   | R1   | R0   | G5   | G4   | G3  | G2  | G1  | G0  | B5  | B4  | B3  | B2  | B1  | B0  | 262K-Color |

Table 4.10: 18-bit parallel interface type II GRAM write set table

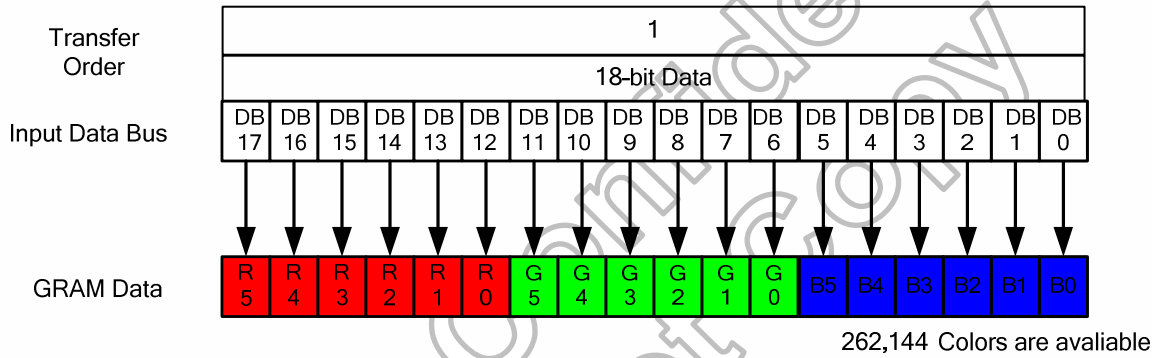


**18-bit parallel bus system interface**

The I80-system 18-bit parallel bus interface **type I** in command-parameter interface mode can be used by setting external pins “IM3, IM2, IM1, IM0” pins to “1000”. And the I80-system 18-bit parallel bus interface **type II** in command-parameter interface mode can be used by setting “IM3, IM2, IM1, IM0” pins to “1010”. Figure 4.3 is the example of interface with I80 microcomputer system interface.



**Figure 4.3: Example of I80- system 18-bit parallel bus interface**



**Figure 4.4: Input data bus and GRAM data mapping in 18-bit bus system interface with 18-bit-data Input (“IM3, IM2, IM1, IM0”=“1010” or “1000”)**

**16-bit parallel bus system interface**

The I80-system 16-bit parallel bus interface **type I** in command-parameter interface mode can be used by setting external pins “IM3, IM2, IM1, IM0” pins to “0000”. And I80-system 16-bit parallel bus interface **type II** in command-parameter interface mode can be used by setting “IM3, IM2, IM1, IM0” pins to “0010”. Figure 4.5 is the example of type I interface with I80 microcomputer system interface. And Figure 4.6 is the example of type II interface with I80 microcomputer system interface.

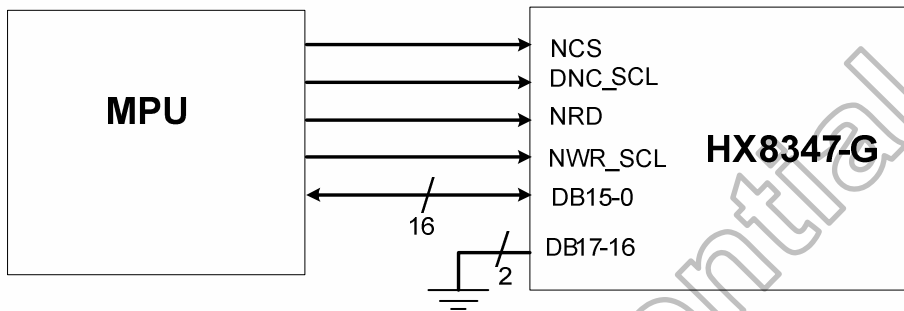


Figure 4.5: Example of I80 system 16-bit parallel bus interface type I

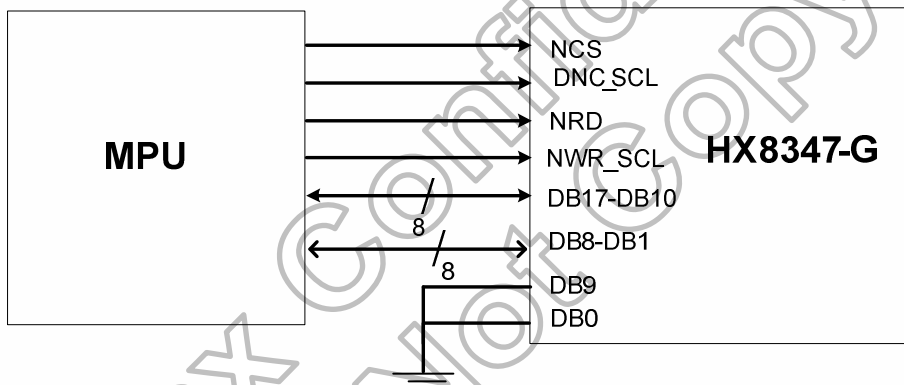


Figure 4.6: Example of I80 system 16-bit parallel bus interface type II

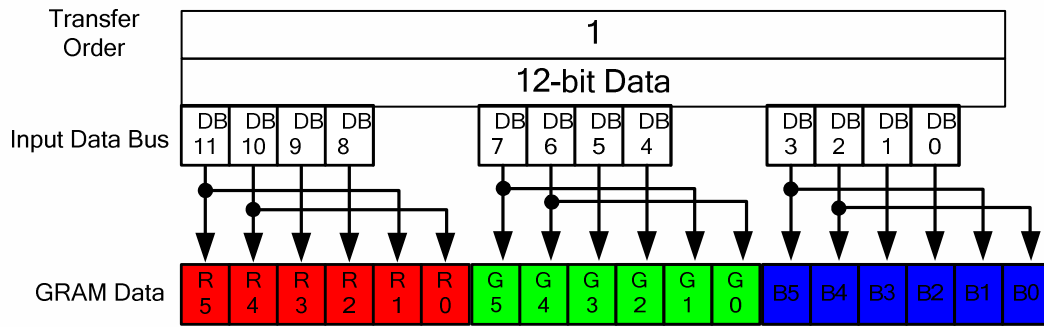


Figure 4.7: Input data bus and GRAM data mapping in 16-bit bus system interface with 12-bit-data input (R17H=03h and “IM3, IM2, IM1, IM0”=”0000”)

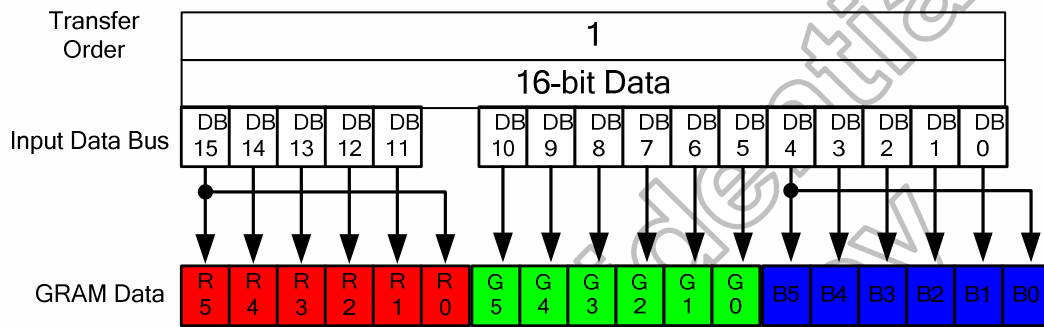


Figure 4.8: Input data bus and GRAM data mapping in 16-bit bus system interface with 16-bit-data input (R17H=05h and “IM3, IM2, IM1, IM0”=”0000”)

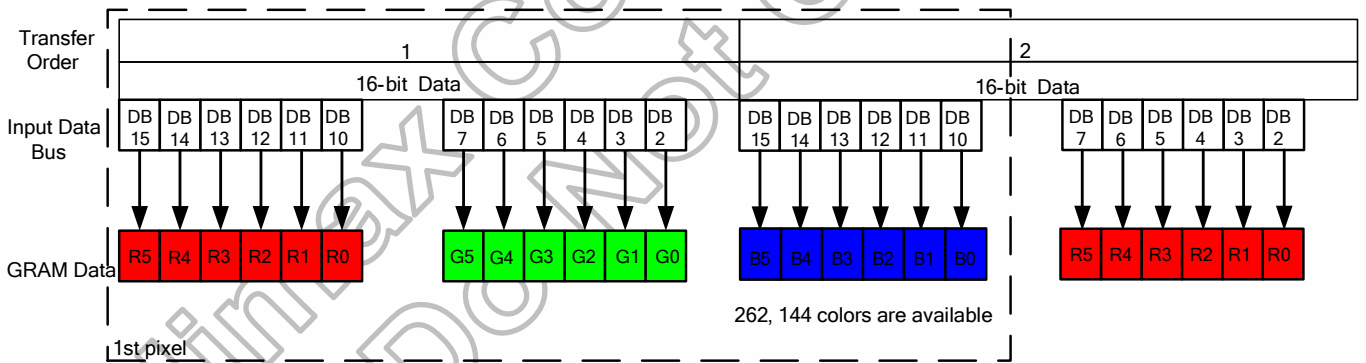


Figure 4.9: Input data bus and GRAM data mapping in 16-bit bus system interface with 18-bit-data input (R17H=06h and “IM3, IM2, IM1, IM0”=”0000”)

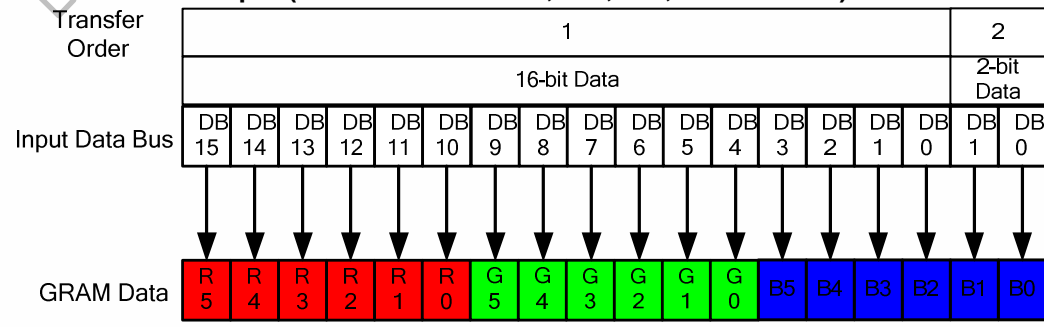


Figure 4.10: Input data bus and GRAM data mapping in 16-bit bus system interface with 18(16+2) bit-data input (R17H=07h and “IM3, IM2, IM1, IM0”=”0000”)

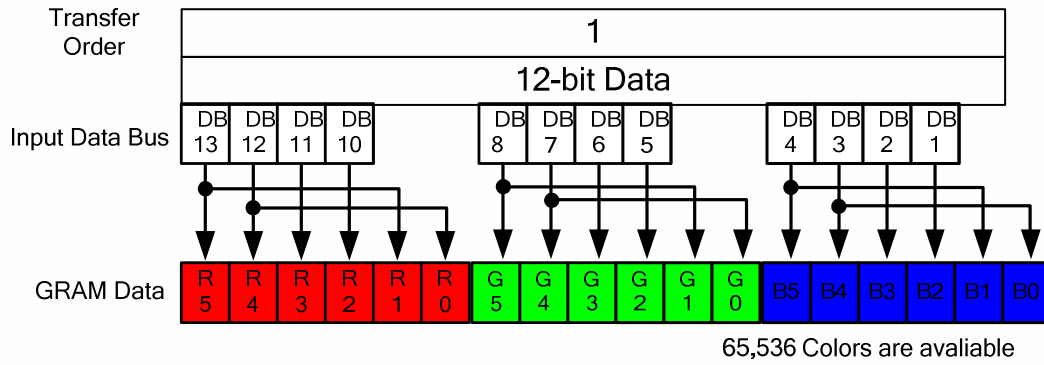


Figure 4.11: Input data bus and GRAM data mapping in 16-bit bus system interface with 12-bit-data input (R17H=03h and "IM3, IM2, IM1, IM0"="0010")

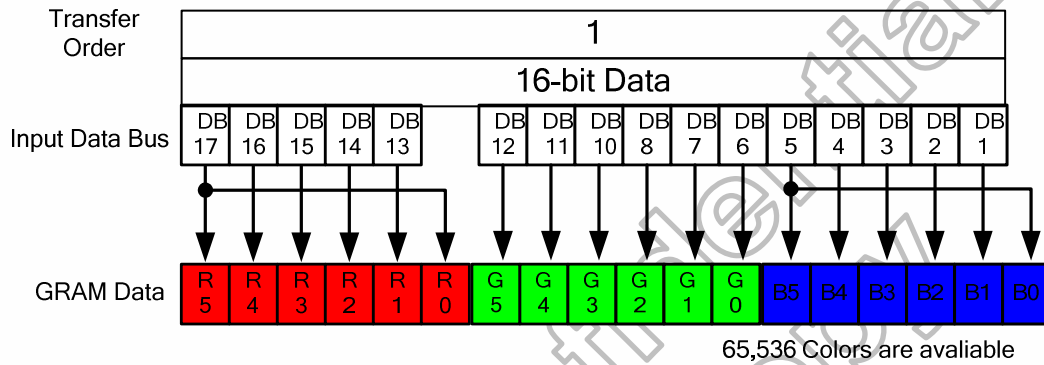


Figure 4.12: Input data bus and GRAM data mapping in 16-bit bus system interface with 16-bit-data input (R17H=05h and "IM3, IM2, IM1, IM0"="0010")

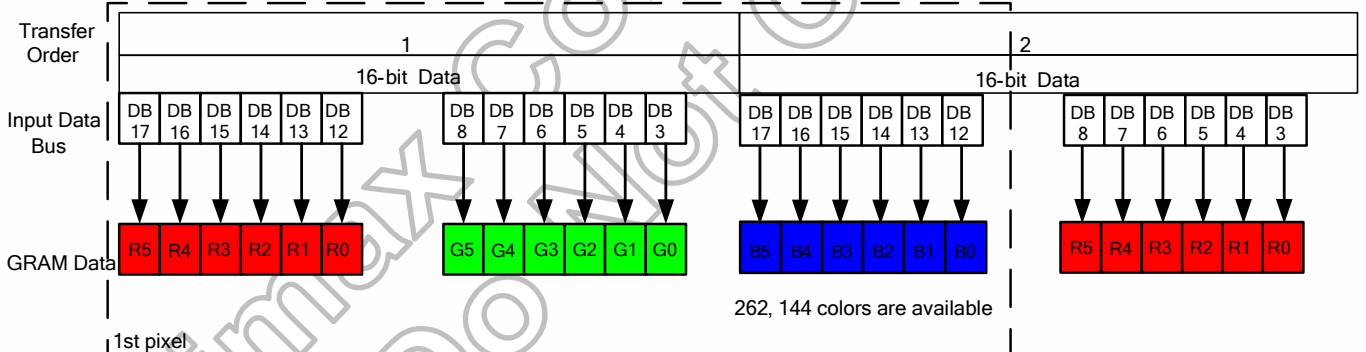


Figure 4.13: Input data bus and GRAM data mapping in 16-bit bus system interface with 18(12+6) bit-data input (R17H=06h and "IM3, IM2, IM1, IM0"="0010")

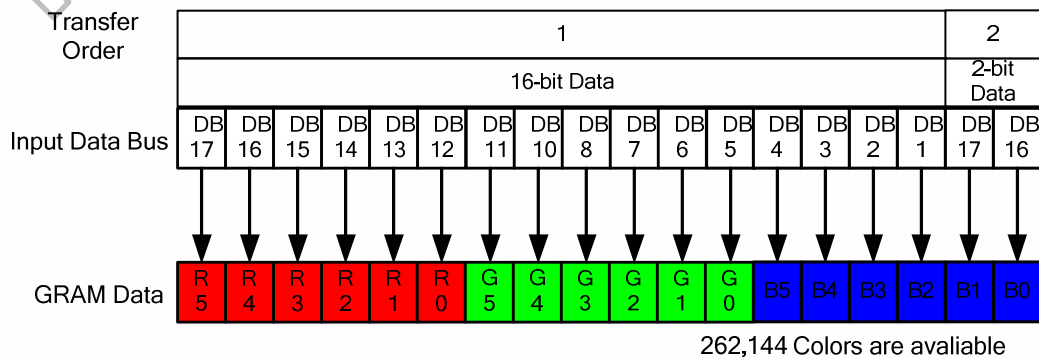


Figure 4.14: Input data bus and GRAM data mapping in 16-bit bus system interface with 18(16+2) bit-data input (R17H=07h and "IM3, IM2, IM1, IM0"="0010")

**9-bit parallel bus system interface**

The I80-system 9-bit parallel bus interface **type I** in command-parameter interface mode can be used by setting external pins “IM3, IM2, IM1, IM0” pins to “1001”. And I80-system 9-bit parallel bus interface **type II** in command-parameter interface mode can be used by setting “IM3, IM2, IM1, IM0” pins to “1011”. Figure 4.15 is the example of type I interface with I80 microcomputer system interface. And Figure 4.16 is the example of type II interface with I80 microcomputer system interface.

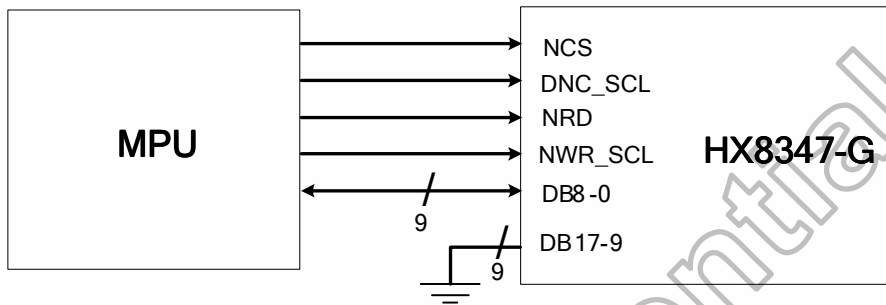


Figure 4.15: Example of I80 system 9-bit parallel bus interface type I

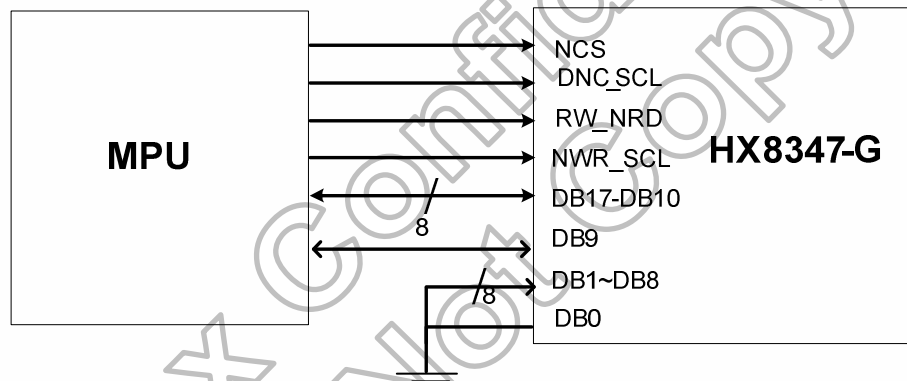


Figure 4.16: Example of I80 system 9-bit parallel bus interface type II



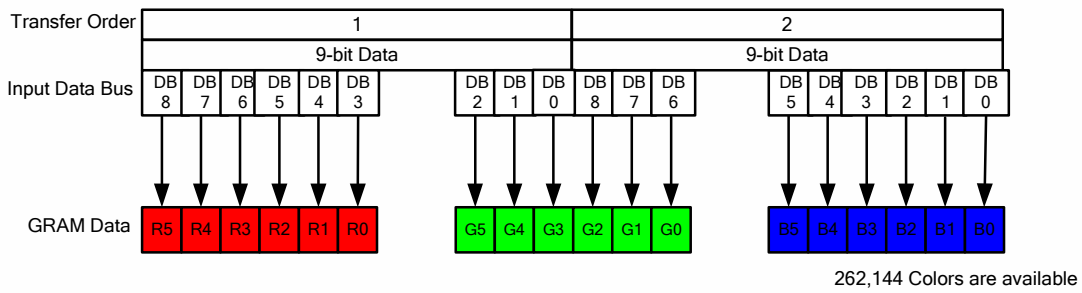


Figure 4.17: Input data bus and GRAM data mapping in 9-bit bus system interface with 18-bit-data input (R17H=06h and “IM3, IM2, IM1, IM0”=“1001”)

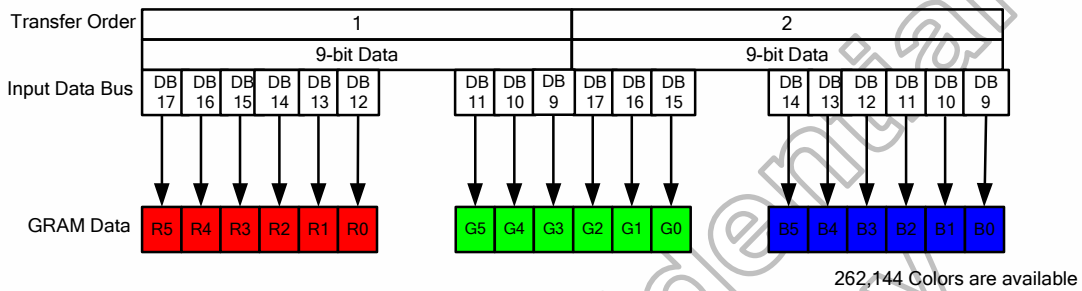


Figure 4.18: Input data bus and GRAM data mapping in 9-bit bus system interface with 18-bit-data input (R17H=06h and “IM3, IM2, IM1, IM0”=“1011”)

**8-bit Parallel Bus System Interface**

The I80-system 8-bit parallel bus interface **type I** in command-parameter interface mode can be used by setting external pins “IM3, IM2, IM1, IM0” pins to “0001”. And I80-system 8-bit parallel bus interface **type II** in command-parameter interface mode can be used by setting “IM3, IM2, IM1, IM0” pins to “0011”. Figure 4.19 is the example of type I interface with I80 microcomputer system interface. And Figure 4.20 is the example of type II interface with I80 microcomputer system interface.

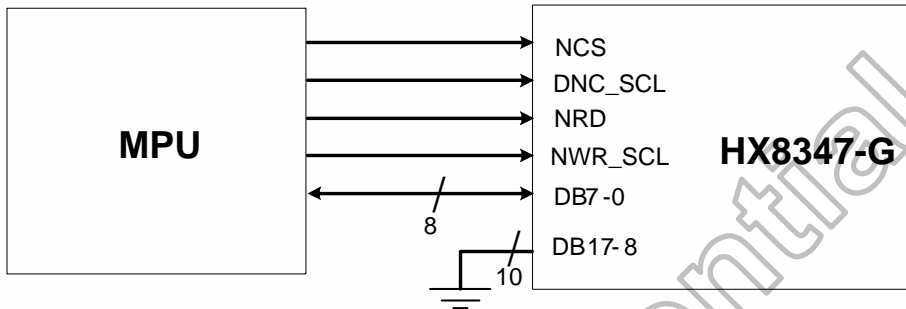


Figure 4.19: Example of I80 system 8-bit parallel bus interface type I

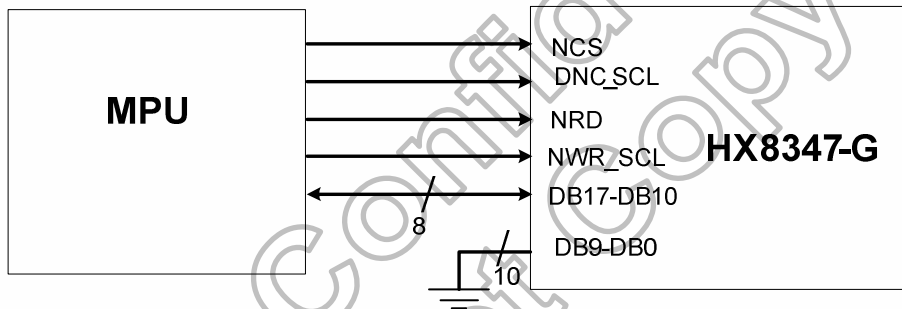


Figure 4.20: Example of I80 system 8-bit parallel bus interface type II

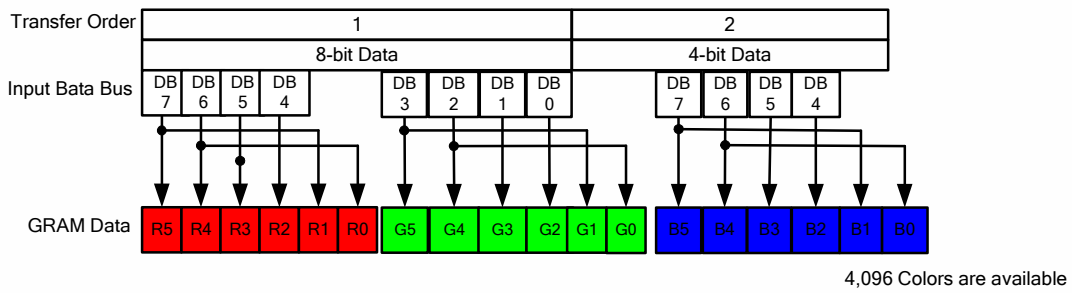


Figure 4.21: Input data bus and GRAM data mapping in 8-bit bus system interface with 12-bit-data input (R17H=03h and “IM3, IM2, IM1, IM0”=“0001”)

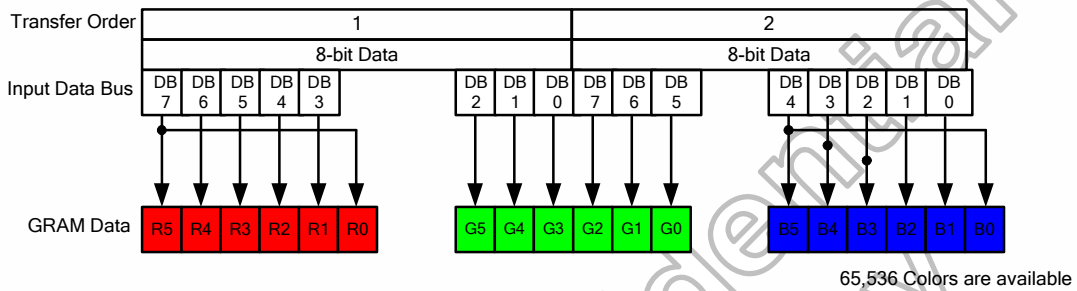


Figure 4.22: Input data bus and GRAM data mapping in 8-bit bus system interface with 16-bit-data input (R17H=05h and “IM3, IM2, IM1, IM0”=“0001”)

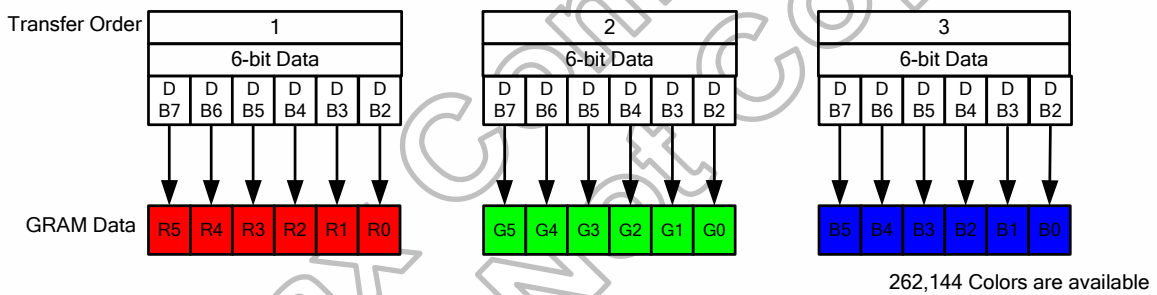
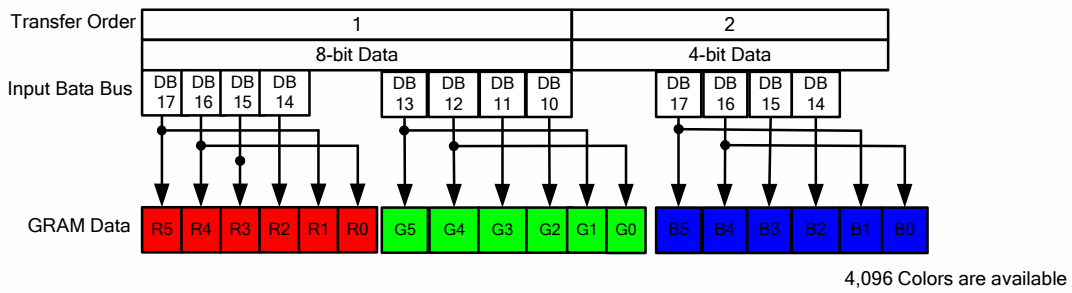
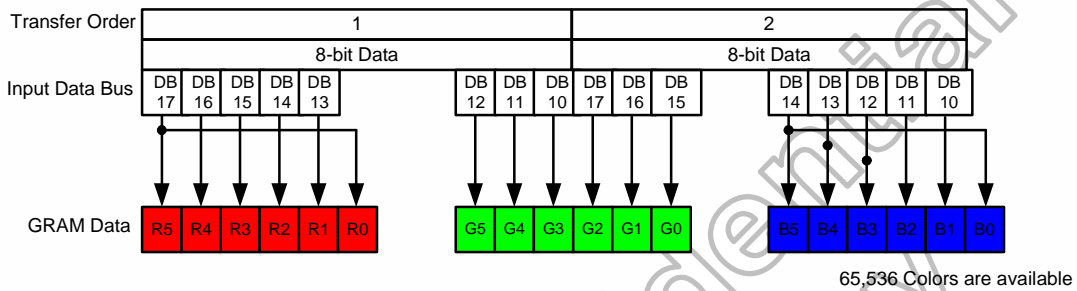


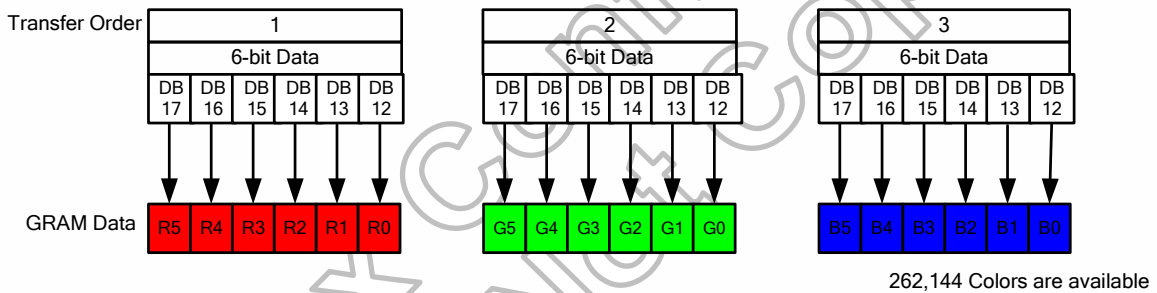
Figure 4.23: Input data bus and GRAM data mapping in 8-bit bus system interface with 18-bit-data input (R17H=06h and “IM3, IM2, IM1, IM0”=“0001”)



**Figure 4.24: Input data bus and GRAM data mapping in 8-bit bus system interface with 12-bit-data input (R17H=03h and “IM3, IM2, IM1, IM0”=“0011”)**



**Figure 4.25: Input data bus and GRAM data mapping in 8-bit bus system interface with 16-bit-data input (R17H=05h and “IM3, IM2, IM1, IM0”=“0011”)**



**Figure 4.26: Input data bus and GRAM data mapping in 8-bit bus system interface with 18-bit-data input (R17H=06h and “IM3, IM2, IM1, IM0”=“0011”)**

## MCU Data Color Coding for RAM data Read

- Parallel 8-Bit Bus Interface type I (IM3,IM2,IM1,IM0="0001")

| Register Command | D17 | D16 | D15 | D14 | D13 | D12 | D11 | D10 | D9 | D8 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | Command                         |
|------------------|-----|-----|-----|-----|-----|-----|-----|-----|----|----|----|----|----|----|----|----|----|----|---------------------------------|
|                  | x   | x   | x   | x   | x   | x   | x   | x   | x  | x  | 0  | 0  | 1  | 0  | 0  | 0  | 1  | 0  | <b>22H</b>                      |
| Read Data Format | D17 | D16 | D15 | D14 | D13 | D12 | D11 | D10 | D9 | D8 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | Color                           |
|                  | x   | x   | x   | x   | x   | x   | x   | x   | x  | x  | x  | x  | x  | x  | x  | x  | x  | x  | Dummy Read                      |
|                  | x   | x   | x   | x   | x   | x   | x   | x   | x  | x  | R5 | R4 | R3 | R2 | R1 | R0 | x  | x  | 262K-Color<br>(1-pixel/ 3bytes) |
|                  | x   | x   | x   | x   | x   | x   | x   | x   | x  | x  | G5 | G4 | G3 | G2 | G1 | G0 | x  | x  |                                 |
| x                | x   | x   | x   | x   | x   | x   | x   | x   | x  | B5 | B4 | B3 | B2 | B1 | B0 | x  | x  |    |                                 |

Table 4.11: 8-bit parallel interface type I GRAM read table

- Parallel 16-Bit Bus Interface type I (IM3,IM2,IM1,IM0="0000")

| Register Command | D17 | D16 | D15 | D14 | D13 | D12 | D11 | D10 | D9 | D8 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | Command                          |
|------------------|-----|-----|-----|-----|-----|-----|-----|-----|----|----|----|----|----|----|----|----|----|----|----------------------------------|
|                  | x   | x   | x   | x   | x   | x   | x   | x   | x  | x  | 0  | 0  | 1  | 0  | 0  | 0  | 1  | 0  | <b>22H</b>                       |
| Read Data Format | D17 | D16 | D15 | D14 | D13 | D12 | D11 | D10 | D9 | D8 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | Color                            |
|                  | x   | x   | x   | x   | x   | x   | x   | x   | x  | x  | x  | x  | x  | x  | x  | x  | x  | x  | Dummy Read                       |
|                  | x   | x   | R5  | R4  | R3  | R2  | R1  | R0  | x  | x  | G5 | G4 | G3 | G2 | G1 | G0 | x  | x  | 262K-Color<br>(2-pixels/ 3bytes) |
|                  | x   | x   | B5  | B4  | B3  | B2  | B1  | B0  | x  | x  | R5 | R4 | R3 | R2 | R1 | R0 | x  | x  |                                  |
| x                | x   | G5  | G4  | G3  | G2  | G1  | G0  | x   | x  | B5 | B4 | B3 | B2 | B1 | B0 | x  | x  |    |                                  |

Table 4.12: 16-bit parallel interface type I GRAM read table

- Parallel 9-Bit Bus Interface type I (IM3,IM2,IM1,IM0="1001")

| Register Command | D17 | D16 | D15 | D14 | D13 | D12 | D11 | D10 | D9 | D8 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | Register                        |
|------------------|-----|-----|-----|-----|-----|-----|-----|-----|----|----|----|----|----|----|----|----|----|----|---------------------------------|
|                  | x   | x   | x   | x   | x   | x   | x   | x   | x  | x  | 0  | 0  | 1  | 0  | 0  | 0  | 1  | 0  | <b>22H</b>                      |
| Read Data Format | D17 | D16 | D15 | D14 | D13 | D12 | D11 | D10 | D9 | D8 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | Color                           |
|                  | x   | x   | x   | x   | x   | x   | x   | x   | x  | x  | x  | x  | x  | x  | x  | x  | x  | x  | Dummy Read                      |
|                  | x   | x   | x   | x   | x   | x   | x   | x   | x  | R5 | R4 | R3 | R2 | R1 | R0 | G5 | G4 | G3 | 262K-Color<br>(1-pixel/ 2bytes) |
|                  | x   | x   | x   | x   | x   | x   | x   | x   | x  | G2 | G1 | G0 | B5 | B4 | B3 | B2 | B1 | B0 |                                 |

Table 4.13: 9-bit parallel interface type I GRAM read table

- Parallel 18-Bit Bus Interface type I (IM3,IM2,IM1,IM0="1000")

| Register Command | D17 | D16 | D15 | D14 | D13 | D12 | D11 | D10 | D9 | D8 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | Register   |
|------------------|-----|-----|-----|-----|-----|-----|-----|-----|----|----|----|----|----|----|----|----|----|----|------------|
|                  | x   | x   | x   | x   | x   | x   | x   | x   | x  | x  | 0  | 0  | 1  | 0  | 0  | 0  | 1  | 0  | <b>22H</b> |
| Read Data Format | D17 | D16 | D15 | D14 | D13 | D12 | D11 | D10 | D9 | D8 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | Color      |
|                  | x   | x   | x   | x   | x   | x   | x   | x   | x  | x  | x  | x  | x  | x  | x  | x  | x  | x  | Dummy Read |
|                  | R5  | R4  | R3  | R2  | R1  | R0  | G5  | G4  | G3 | G2 | G1 | G0 | B5 | B4 | B3 | B2 | B1 | B0 | 262K-Color |
|                  |     |     |     |     |     |     |     |     |    |    |    |    |    |    |    |    |    |    |            |

Table 4.14: 18-bit parallel interface type I GRAM read table



- Parallel 8-Bit Bus Interface type II (IM3,IM2,IM1,IM0="0011")

| Register Command | DB17 | DB16 | DB15 | DB14 | DB13 | DB12 | DB11 | DB10 | DB9 | DB8 | DB7 | DB6 | DB5 | DB4 | DB3 | DB2 | DB1 | DB0 | Command                         |
|------------------|------|------|------|------|------|------|------|------|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|---------------------------------|
|                  | 0    | 0    | 1    | 0    | 0    | 0    | 1    | 0    | x   | x   | x   | x   | x   | x   | x   | x   | x   | x   | <b>22H</b>                      |
| Read Data Format | DB17 | DB16 | DB15 | DB14 | DB13 | DB12 | DB11 | DB10 | DB9 | DB8 | DB7 | DB6 | DB5 | DB4 | DB3 | DB2 | DB1 | DB0 | Color                           |
|                  | x    | x    | x    | x    | x    | x    | x    | x    | x   | x   | x   | x   | x   | x   | x   | x   | x   | x   | Dummy Read                      |
|                  | R5   | R4   | R3   | R2   | R1   | R0   | x    | x    |     |     |     |     |     |     |     |     |     |     | 262K-Color<br>(1-pixel/ 3bytes) |
|                  | G5   | G4   | G3   | G2   | G1   | G0   | x    | x    | x   | x   | x   | x   | x   | x   | x   | x   | x   | x   |                                 |
|                  | B5   | B4   | B3   | B2   | B1   | B0   | x    | x    | x   | x   | x   | x   | x   | x   | x   | x   | x   | x   |                                 |

Table 4.15: 8-bit parallel interface type II GRAM read table

- Parallel 16-Bit Bus Interface type II (IM3,IM2,IM1,IM0="0010")

| Register Command | DB17 | DB16 | DB15 | DB14 | DB13 | DB12 | DB11 | DB10 | DB9 | DB8 | DB7 | DB6 | DB5 | DB4 | DB3 | DB2 | DB1 | DB0 | Command                          |
|------------------|------|------|------|------|------|------|------|------|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|----------------------------------|
|                  | x    | x    | x    | x    | x    | x    | x    | x    | x   | 0   | 0   | 1   | 0   | 0   | 0   | 1   | 0   | x   | <b>22H</b>                       |
| Read Data Format | DB17 | DB16 | DB15 | DB14 | DB13 | DB12 | DB11 | DB10 | DB9 | DB8 | DB7 | DB6 | DB5 | DB4 | DB3 | DB2 | DB1 | DB0 | Color                            |
|                  |      | x    | x    | x    | x    | x    | x    | x    | x   |     | x   | x   | x   | x   | x   | x   | x   | x   | Dummy Read                       |
|                  | R5   | R4   | R3   | R2   | R1   | R0   | x    | x    | x   | G5  | G4  | G3  | G2  | G1  | G0  | x   | x   | x   | 262K-Color<br>(2-pixels/ 3bytes) |
|                  | B5   | B4   | B3   | B2   | B1   | B0   | x    | x    | x   | R5  | R4  | R3  | R2  | R1  | R0  | x   | x   | x   |                                  |
|                  | G5   | G4   | G3   | G2   | G1   | G0   | x    | x    | x   | B5  | B4  | B3  | B2  | B1  | B0  | x   | x   | x   |                                  |

Table 4.16: 16-bit parallel interface type II GRAM read table

- Parallel 9-Bit Bus Interface type II (IM3,IM2,IM1,IM0="1011")

| Register Command | D17 | D16 | D15 | D14 | D13 | D12 | D11 | D10 | D9 | D8 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | Register                        |
|------------------|-----|-----|-----|-----|-----|-----|-----|-----|----|----|----|----|----|----|----|----|----|----|---------------------------------|
|                  | 0   | 0   | 1   | 0   | 0   | 0   | 1   | 0   | x  | x  | x  | x  | x  | x  | x  | x  | x  | x  | <b>22H</b>                      |
| Read Data Format | D17 | D16 | D15 | D14 | D13 | D12 | D11 | D10 | D9 | D8 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | Color                           |
|                  | x   | x   | x   | x   | x   | x   | x   | x   | x  | x  | x  | x  | x  | x  | x  | x  | x  | x  | Dummy Read                      |
|                  | R5  | R4  | R3  | R2  | R1  | R0  | G5  | G4  | G3 | x  | x  | x  | x  | x  | x  | x  | x  | x  | 262K-Color<br>(1-pixel/ 2bytes) |
|                  | G2  | G1  | G0  | B5  | B4  | B3  | B2  | B1  | B0 | x  | x  | x  | x  | x  | x  | x  | x  | x  |                                 |

Table 4.17: 9-bit parallel interface type II GRAM read table

- Parallel 18-Bit Bus Interface type II (IM3,IM2,IM1,IM0="1010")

| Register Command | D17 | D16 | D15 | D14 | D13 | D12 | D11 | D10 | D9 | D8 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | Register   |
|------------------|-----|-----|-----|-----|-----|-----|-----|-----|----|----|----|----|----|----|----|----|----|----|------------|
|                  | x   | x   | x   | x   | x   | x   | x   | x   | x  | 0  | 0  | 1  | 0  | 0  | 0  | 1  | 0  | x  | <b>22H</b> |
| Read Data Format | D17 | D16 | D15 | D14 | D13 | D12 | D11 | D10 | D9 | D8 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | Color      |
|                  | x   | x   | x   | x   | x   | x   | x   | x   | x  | x  | x  | x  | x  | x  | x  | x  | x  | x  | Dummy Read |
|                  | R5  | R4  | R3  | R2  | R1  | R0  | G5  | G4  | G3 | G2 | G1 | G0 | B5 | B4 | B3 | B2 | B1 | B0 | 262K-Color |

Table 4.18: 18-bit parallel interface type II GRAM read table

### 4.1.3 Serial bus system interface

The HX8347-G supports two kinds of serial bus interface in register-content mode by setting external pins “IM3, IM2, IM1” pins to “010” 3-wire serial interface I, and “IM3,IM2, IM1” pins to “011” 4-wire serial interface I. The serial bus system interface I mode is enabled through the chip select line (NCS), and it is accessed via a control consisting of the serial input data (SDA), and the serial transfer clock signal (NWR\_SCL).

The external setting “IM3, IM2, IM1” pins to “110” 3-wire serial interface II and and “IM3,IM2, IM1” pins to “111” 4-wire serial interface II. The serial bus system interface I mode is enabled through the chip select line (NCS), and it is accessed via a control consisting of the serial input data (SDI) output data (SDO), and the serial transfer clock signal (NWR\_SCL).

#### 4.1.3.1 3-wire serial interface

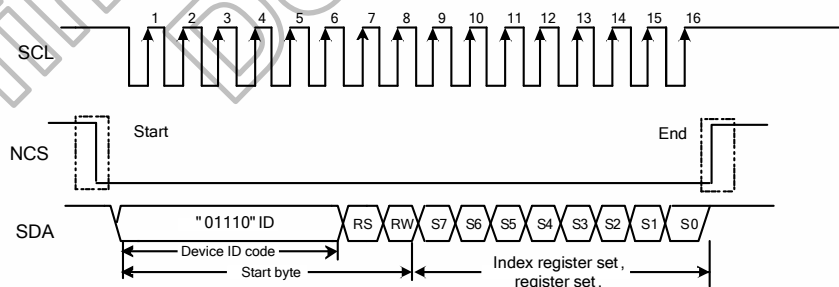
As the chip select signal (NCS) goes low, the start byte needs to be transferred first. The start byte is made up of 6-bit bus device identification code; register select (RS) bit and read/write operation (RW) bit. The five upper bits of 6-bit bus device identification code must be set to “01110”, and the least significant bit of the identification code must be set as the external pin IM0 input as “ID”.

The seventh bit (RS) of the start byte determines internal index register or register, GRAM accessing. RS must be set to “0” when writing data to the index register or reading the status and it must be set to “1” when writing or reading a command or GRAM data. The read or write operation is selected by the eighth bit (RW) of the start byte. The data is written to the chip when R/W = 0, and read from chip when RW = 1.

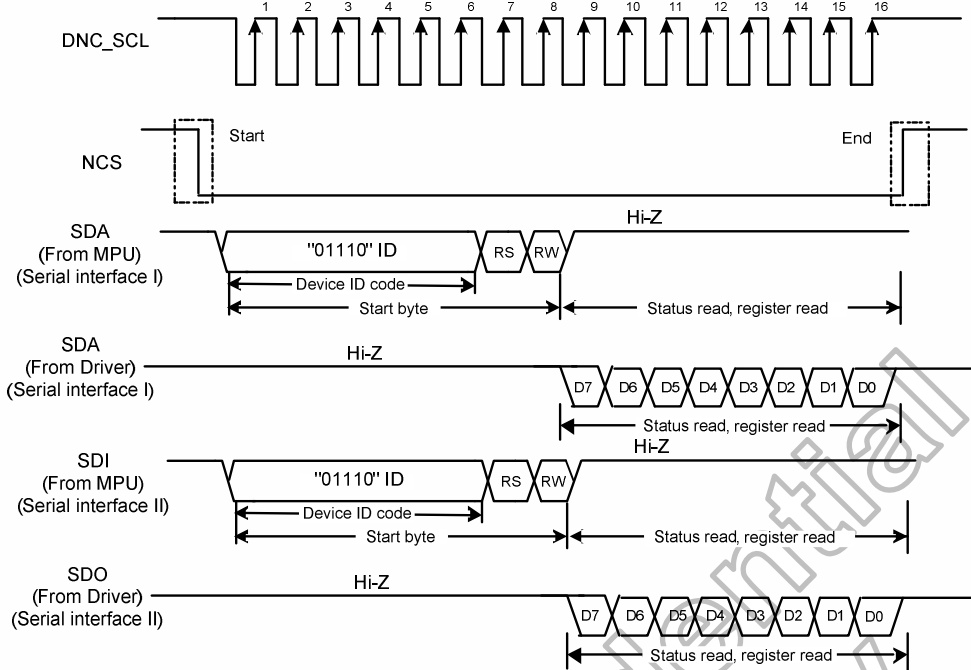
| RS | R/W | Function                              |
|----|-----|---------------------------------------|
| 0  | 0   | Set index register                    |
| 1  | 0   | Writes Instruction or GRAM data       |
| 1  | 1   | Reads command (Not support GRAM read) |

**Table 4.19: Function of RS and R/W bit bus**

#### A) Transfer Timing Format in Serial Bus Interface for Index Register or Register Write



**B) Transfer Timing Format in Serial Bus Interface for Index Register or Register Read**



**Figure 4.27: Index register read/write timing in 3-wire serial bus system interface**

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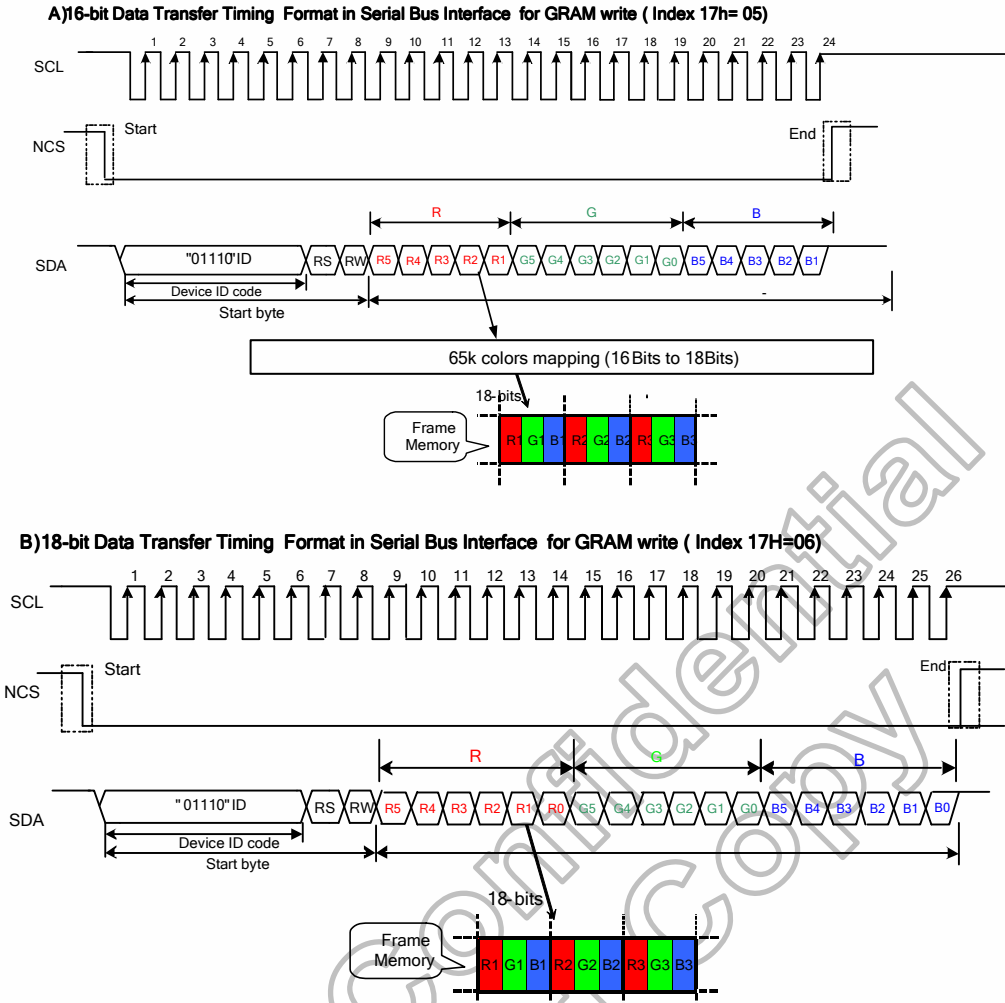


Figure 4.28: Data write timing in 3-wire serial bus system interface

### 4.1.3.2 4-wire serial interface

4-pin serial case, data packet contains just transmission byte and control bit DNC is transferred by DNC pin. If DNC is low, the transmission byte is command byte. If DNC is high, the transmission byte is stored to index register or GRAM. The MSB is transmitted first. The serial interface is initialized when NCS is high. In this state, NWR\_SCL clock pulse or SDA data have no effect. A falling edge on NCS enables the serial interface and indicates the start of data transmission.

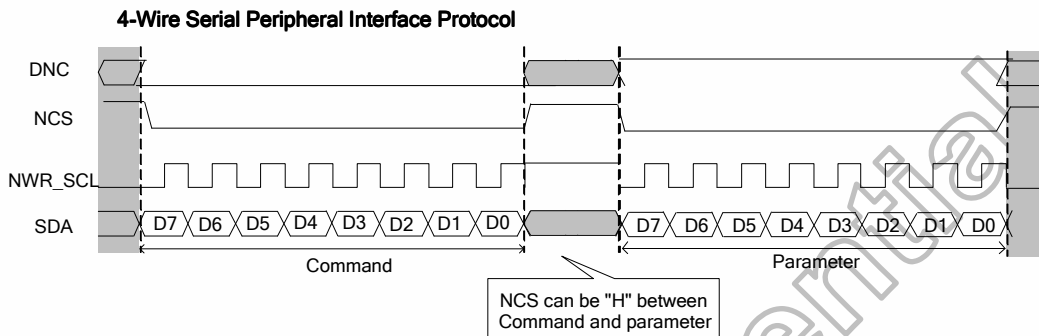


Figure 4.29: Index register write timing in 4-wire serial bus system interface

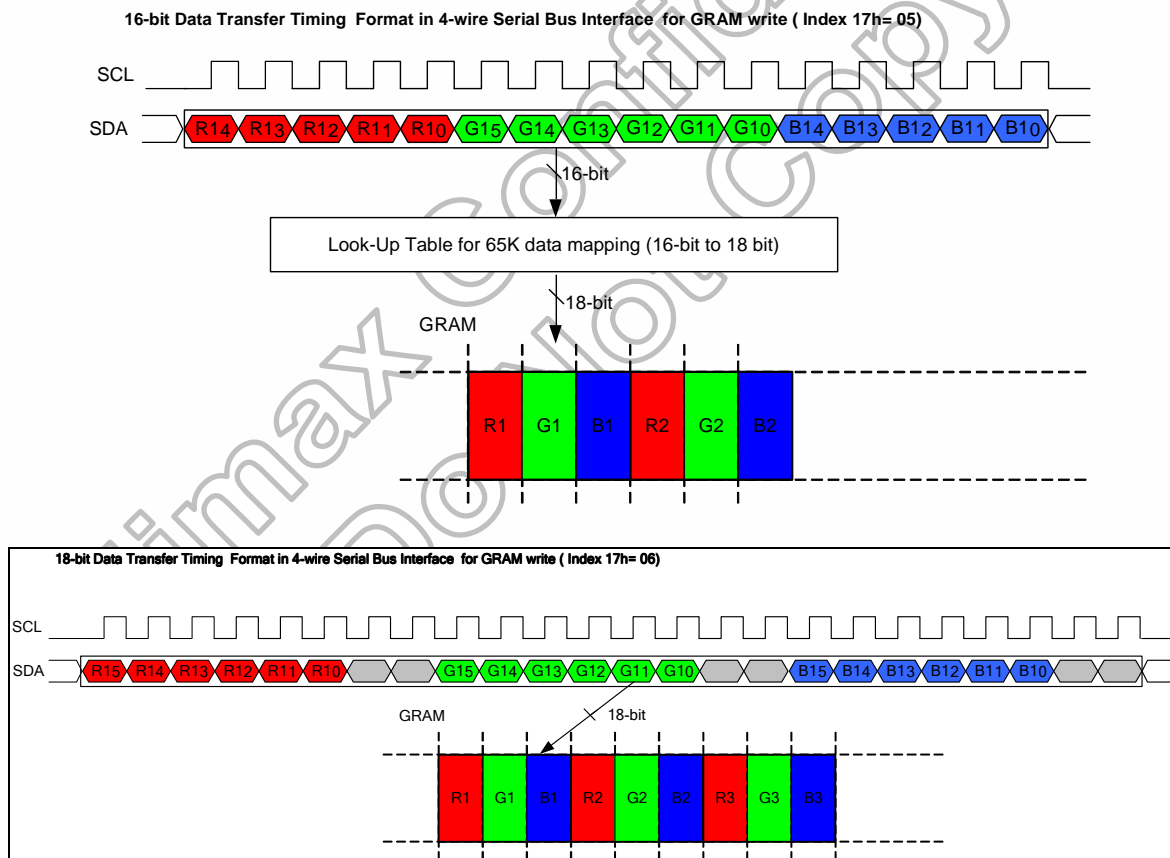


Figure 4.30: Data write timing in 4-wire serial bus system interface

## 4.2 RGB Interface

The HX8347-G uses **RCM [1:0] = '10' or '11' Software setting to select RGB interface**. After Power on Sequence, the RGB interface is activated. When RCM [1:0] = '10' use VSYNC, HSYNC, DE, DOTCLK, DB17-0 parallel lines for the RGB interface (RGB mode 1). When RCM [1:0] = '11' use VSYNC, HSYNC, DOTCLK, DB17-0 parallel lines for the RGB interface (RGB mode 2)

Pixel clock (DOTCLK) must be running all the time without stopping and it is used to entering VSYNC, HSYNC, DE and DB17-0 lines states when there is a rising edge of the DOTCLK.

In RGB interface mode 1, the valid display data is inputted in pixel unit via DB17-0 according to the high-level('H') of DE signal, and display operations are executed in synchronization with the frame synchronizing signal (VSYNC), line synchronizing signal (HSYNC) and pixel clock (DOTCLK). In RGB interface mode 2, the valid display data is inputted in pixel unit via DB17-0 according to the HBP setting of HSYNC signal, and the VBP setting of VSYNC. In these two RGB interface modes, the input display data is not written to GRAM and is displayed directly.

Vertical synchronization (VSYNC) signal is used to tell when there a new frame of the display is received , and this is negative ('-', '0', low) active. Horizontal synchronization signal (HSYNC) is used to tell when a new line of the frame is received, and this is negative ('-', '0', low) active. Data enable (DE) is used to tell when RGB information is received that should be transferred on the display, and this is positive ('+', '1', high) active. DB17-0 are used to tell what the information of the image is, that is transferred on the display when DE='H'.

The pixel clock cycle is described in the following figure.

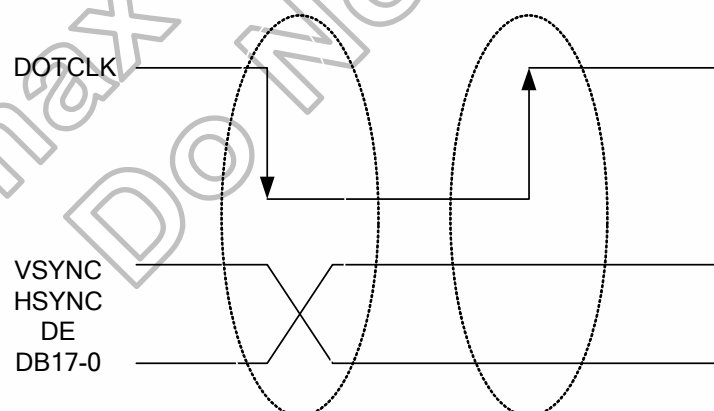
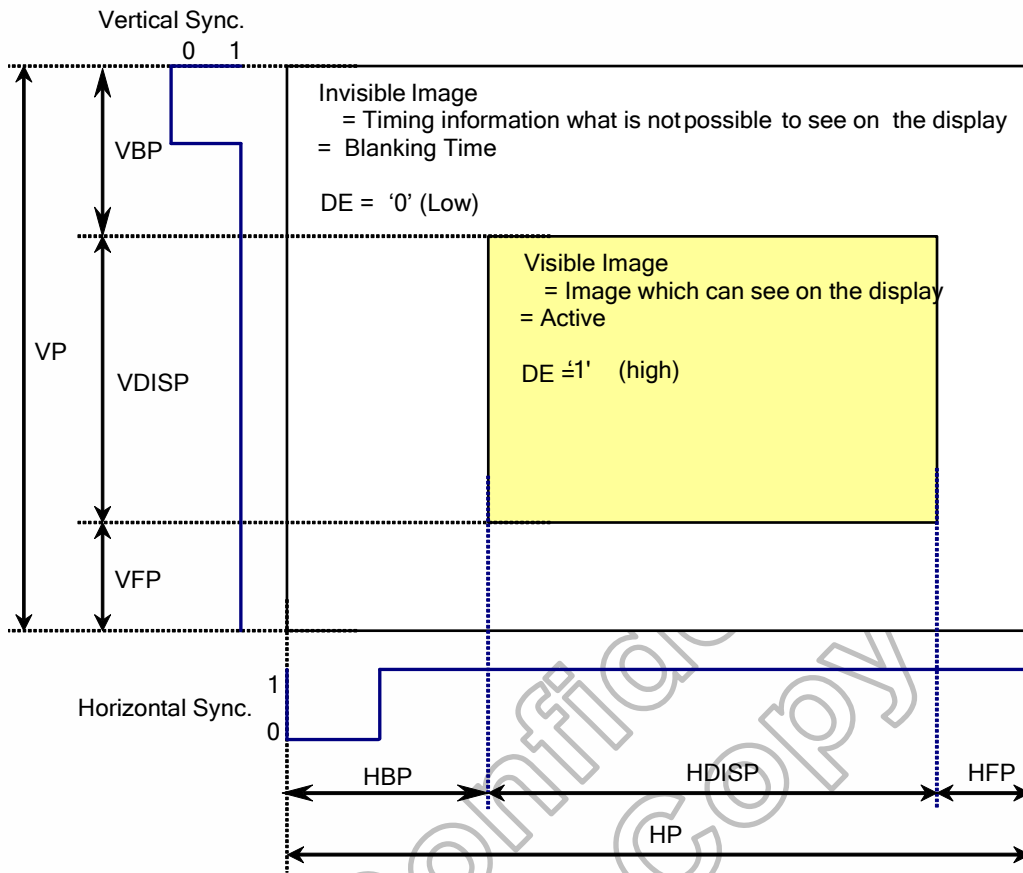


Figure 4.31: DOTCLK cycle

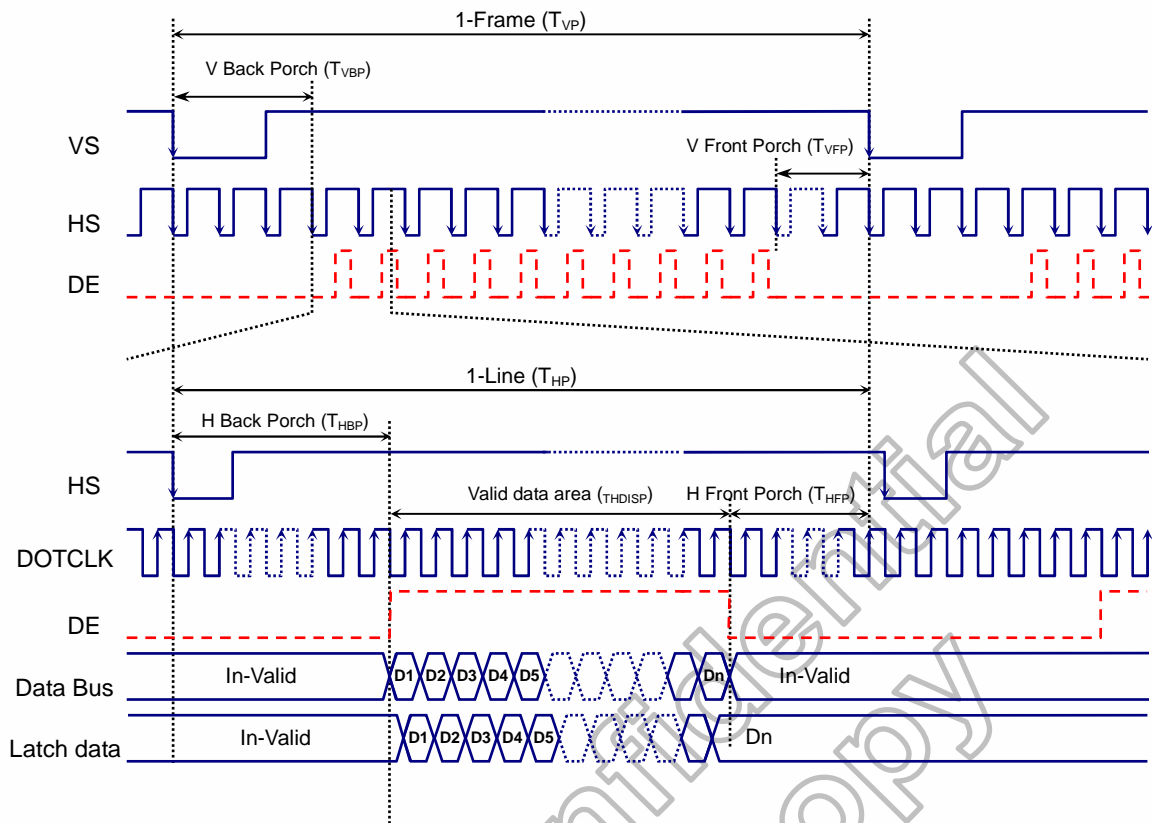


General timing diagram in RGB interface is as follow.



**Figure 4.32: RGB interface circuit input timing diagram**

The image information is correct on the display when the timings are in range on the interface. However, the image information will be incorrect on the display, when timings are out of the range on the RGB interface and the correct image information will be displayed automatically (by the display module) on the next frame (vertical sync.), when there is returned from out of the range to in range RGB interface timings.



**Note:** (1) RGB mode 2 doesn't need DE signal  
 (2) EPL='0', VSPL='0', HSPL='0' and DPL='0' of SETRGBIF (32H) command.

**Figure 4.33: RGB mode timing diagram**

All 3 kinds of bus width can be available during RGB interface mode (selected by COLMOD (17H) command for 6-bit, 16-bit and 18-bit data width)

|     |     |     |     |     |     |     |     |     |    |    |    |    |    |    |    |    |    |    |             |
|-----|-----|-----|-----|-----|-----|-----|-----|-----|----|----|----|----|----|----|----|----|----|----|-------------|
| 17H | D17 | D16 | D15 | D14 | D13 | D12 | D11 | D10 | D9 | D8 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | Bus width   |
| 50h | R4  | R3  | R2  | R1  | R0  | x   | G5  | G4  | G3 | G2 | G1 | G0 | B4 | B3 | B2 | B1 | B0 | x  | 16-bit data |
| 60h | R5  | R4  | R3  | R2  | R1  | R0  | G5  | G4  | G3 | G2 | G1 | G0 | B5 | B4 | B3 | B2 | B1 | B0 | 18-bit data |
| 17H | D17 | D16 | D15 | D14 | D13 | D12 | D11 | D10 | D9 | D8 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | Bus width   |
| E0h | x   | x   | x   | x   | x   | x   | x   | x   | x  | x  | R5 | R4 | R3 | R2 | R1 | R0 | x  | x  | 6-bit data  |
|     | x   | x   | x   | x   | x   | x   | x   | x   | x  | x  | G5 | G4 | G3 | G2 | G1 | G0 | x  | x  |             |
|     | x   | x   | x   | x   | x   | x   | x   | x   | x  | x  | B5 | B4 | B3 | B2 | B1 | B0 | x  | x  |             |

**Note:** (1) When 17H="E0h", 6-bit data width of 3-time transfer is used to transmit 1 pixel data with the 18-bit color depth information.

(2) Only 17H= "50h","60h", "E0h" are valid on RGB I/F, others are invalid.

**Table 4.20: RGB interface bus width set table**

### RGB interface mode

| RGB I/F Mode | DOTCLK | DE       | VS   | HS   | Video Data bus DB [B:0] | Register for Blanking Porch setting |
|--------------|--------|----------|------|------|-------------------------|-------------------------------------|
| RGB Mode 1   | Used   | Used     | Used | Used | Used                    | Not Used                            |
| RGB Mode 2   | Used   | Not Used | Used | Used | Used                    | Used                                |

There are 2 kinds of RGB mode which is selected by RCM1 & RCM0 hardware pins.

**In RGB Mode 1** (RCM1, RCM0 = "10"), writing data to display is done by DOTCLK and Video Data Bus (DB [17:0]), when DE is high state. The external synchronization signals (DOTCLK, VS and HS) are used for internal display signals. So, controller (host) must always transfer DOTCLK, VS, HS and DE signals to driver.

**In RGB Mode 2** (RCM1, RCM0 = "11"), blanking porch setting of VS and HS signals are defined by R33h and R34h command. DE pin is not used.

#### 4.2.1 Color order on RGB interface

The meaning of the pixel information, when 3 components/pixel (Red, Green and Blue) on RGB interface are used, is described on the following table:

| Pixel Color    | R Component    | G Component    | B Component    |
|----------------|----------------|----------------|----------------|
| <b>Black</b>   | All bits are 0 | All bits are 0 | All bits are 0 |
| <b>Blue</b>    | All bits are 0 | All bits are 0 | All bits are 1 |
| <b>Green</b>   | All bits are 0 | All bits are 1 | All bits are 0 |
| <b>Cyan</b>    | All bits are 0 | All bits are 1 | All bits are 1 |
| <b>Red</b>     | All bits are 1 | All bits are 0 | All bits are 0 |
| <b>Magenta</b> | All bits are 1 | All bits are 0 | All bits are 1 |
| <b>Yellow</b>  | All bits are 1 | All bits are 1 | All bits are 0 |
| <b>White</b>   | All bits are 1 | All bits are 1 | All bits are 1 |

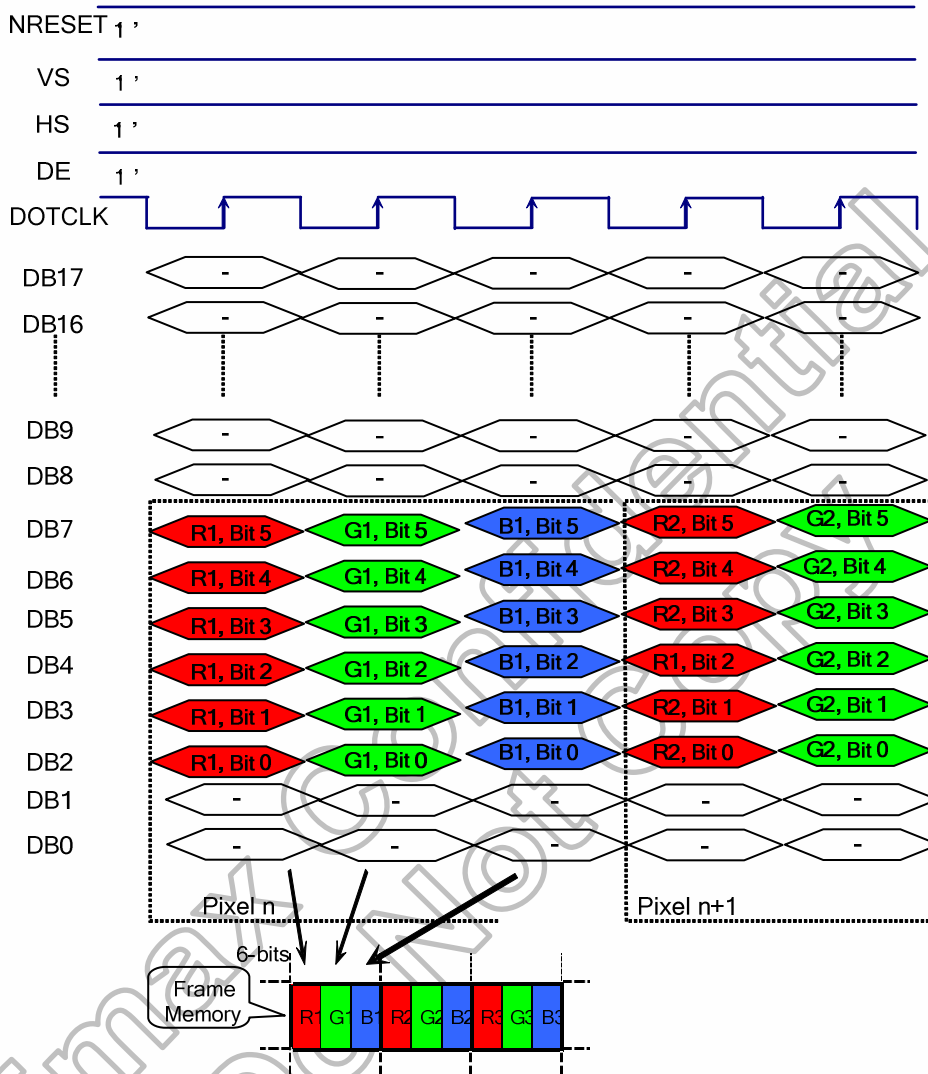
Note: There are only defined main colors on this table - Not all gray levels of colors.

**Table 4.21: Meaning of pixel information for main colors on RGB interface**

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**4.2.2 RGB data color coding**

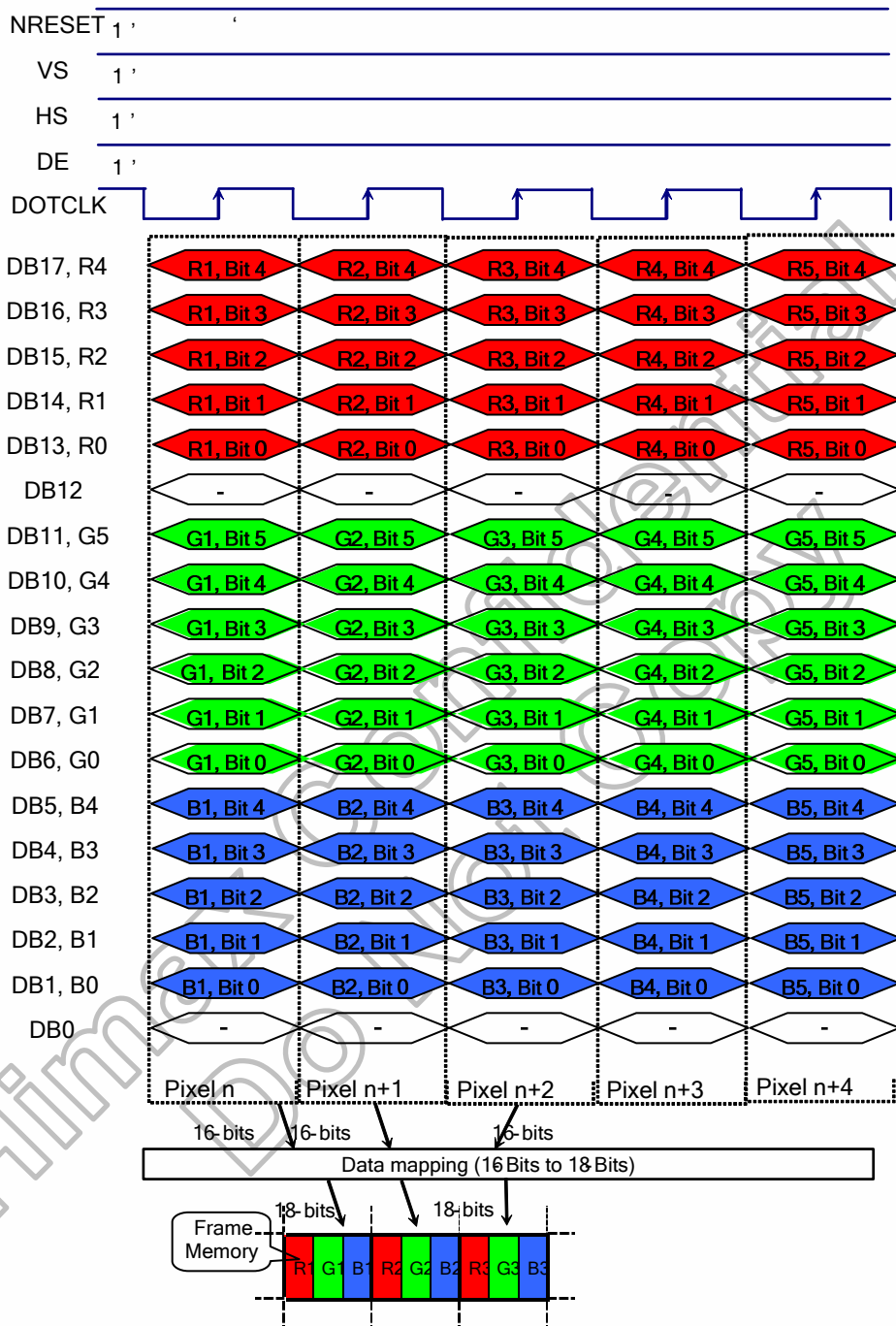
18-bits/pixel Colors Order on 6-bit Data width RGB Interface (RGB 6-6-6-bit input).  
 There is 1 pixel (3 sub-pixels) per 3 bytes, 262K-colors, 17H="E0h"



**Note:** (1) The data order is as follows, MSB=D7, LSB=D0 and picture data is MSB=Bit7, LSB=Bit0 for Red, Green and Blue data. (3-transfer data one pixel)

**Figure 4.34: RGB 18-bit/pixel on 6-bit data width**

16-bits/pixel Colors Order on the 16-bits Data width RGB Interface (RGB 5-6-5-bits input). There is 1 pixel (3 sub-pixels) per byte, 65K-colors, 17H="50h"

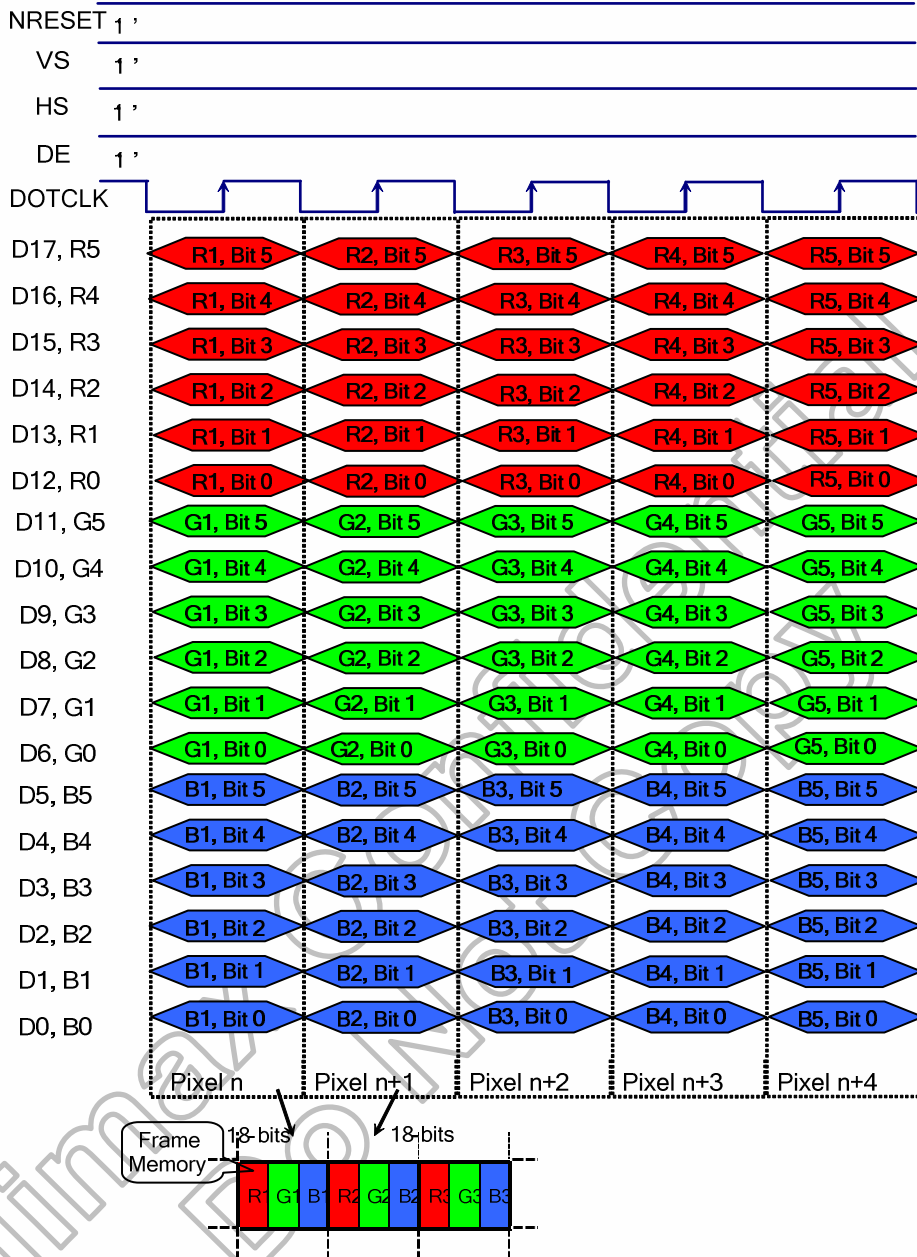


**Note:** (1) The data order is as follows, MSB=D17, LSB=D0 and picture data is MSB=Bit5, LSB=Bit0 for Green data and MSB=Bit4, LSB=Bit0 for Red and Blue data.

**Figure 4.35: RGB 16-bit/pixel on 16-bit data width**



18-bits/pixel Colors Order on the 18-bit Data width RGB Interface (RGB 6-6-6-bit input). There is 1 pixel (3 sub-pixels) per byte, 262K-colors, 17H="60h"



**Note:** (1) The data order is as follows, MSB=D17, LSB=D0 and picture data is MSB=Bit5, LSB=Bit0 for Red, Green and Blue data.

**Figure 4.36: RGB 18-bit/pixel on 18-bit data width**

## 5. Function Description

### 5.1 Display data GRAM mapping

The display data RAM stores display dots and consists of 1,382,400 bits (240x18x320 bits). There is no restriction on access to the RAM even when the display data on the same address is loaded to DAC. There will be no abnormal visible effect on the display when there is a simultaneous Panel Read and Interface Read or Write to the same location of the Frame Memory.

Every pixel (18-bit) data in GRAM is located by a (Page, Column) address (Y, X). By specifying the arbitrary window address **SC**, **EC** bits and **SP**, **EP** bits, it is possible to access the GRAM by setting RAMWR or RAMRD commands from start positions of the window address.

|           |           |           |       |           |           |           |           |
|-----------|-----------|-----------|-------|-----------|-----------|-----------|-----------|
| (00,00)H  | (00,01)H  | (00,02)H  | ----- | (00,EC)H  | (00,ED)H  | (00,EE)H  | (00,EF)H  |
| (01,00)H  | (01,01)H  | (01,02)H  | ----- | (01,EC)H  | (01,ED)H  | (01,EE)H  | (01,EF)H  |
| (02,00)H  | (02,01)H  | (02,02)H  | ----- | (02,EC)H  | (02,ED)H  | (02,EE)H  | (02,EF)H  |
| (03,00)H  | (03,01)H  | (03,02)H  | ----- | (03,EC)H  | (03,ED)H  | (03,EE)H  | (03,EF)H  |
| (04,00)H  | (04,01)H  | (04,02)H  | ----- | (04,EC)H  | (04,ED)H  | (04,EE)H  | (04,EF)H  |
| (05,00)H  | (05,01)H  | (05,02)H  | ----- | (05,EC)H  | (05,ED)H  | (05,EE)H  | (05,EF)H  |
| ⋮         | ⋮         | ⋮         | ⋮     | ⋮         | ⋮         | ⋮         | ⋮         |
| (13A,00)H | (13A,01)H | (13A,02)H | ----- | (13A,EC)H | (13A,ED)H | (13A,EE)H | (13A,EF)H |
| (13B,00)H | (13B,01)H | (13B,02)H | ----- | (13B,EC)H | (13B,ED)H | (13B,EE)H | (13B,EF)H |
| (13C,00)H | (13C,01)H | (13C,02)H | ----- | (13C,EC)H | (13C,ED)H | (13C,EE)H | (13C,EF)H |
| (13D,00)H | (13D,01)H | (13D,02)H | ----- | (13D,EC)H | (13DED)H  | (13D17E)H | (13D,EF)H |
| (13E,00)H | (13E,01)H | (13E,02)H | ----- | (13E,EC)H | (13E,ED)H | (13E,EE)H | (13E,EF)H |
| (13F,00)H | (13F,01)H | (13F,02)H | ----- | (13F,EC)H | (13F,ED)H | (13F,EE)H | (13F,EF)H |

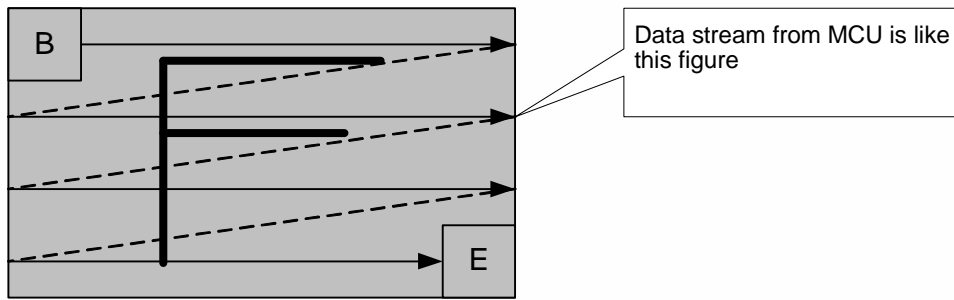
Table 5.1: GRAM address for display panel position

### 5.2 Address Counter (AC) of GRAM

The HX8347-G contains an address counter (AC) which assigns address for writing/reading pixel data to/from GRAM. The address pointers set the position of GRAM. Every time when a pixel data is written into the GRAM, the X address or Y address of AC will be automatically increased by 1 (or decreased by 1), which is decided by the register (**MV**, **MX** and **MY** bits) setting.

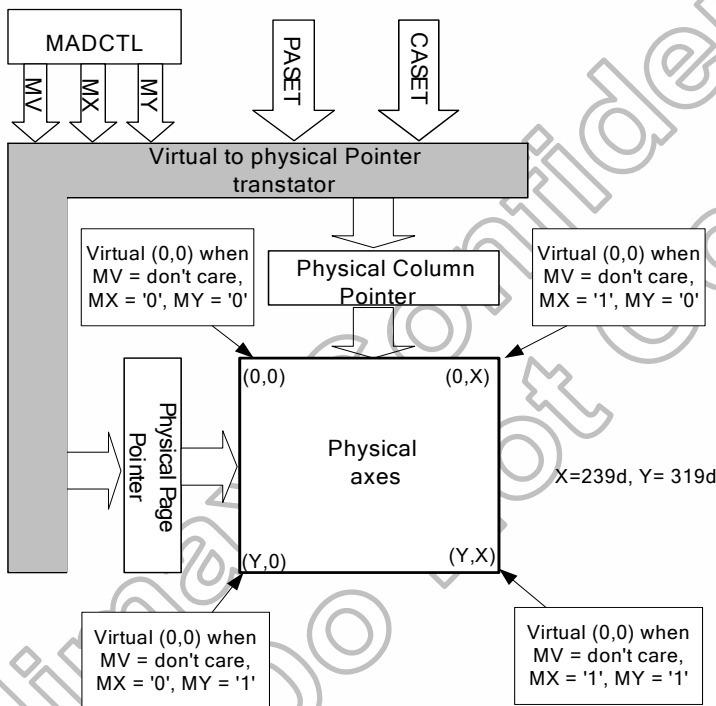
To simplify the address control of GRAM access, the window address function allows for writing data only to a window area of GRAM specified by registers. After data being written to the GRAM, the AC will be increased or decreased within setting window address-range which is specified by the (start: **SC**, end: **EC**) and the (start: **SP**, end: **EP**). Therefore, the data can be written consecutively without thinking a data wrap by those bit function.

**5.2.1 System interface to GRAM write direction**



**Figure 5.1: Image data sending order from host**

The data is written in the order illustrated above. The counter which dictates where in the physical memory the data is to be written is controlled by **MV**, **MX** and **MY** bits setting



**Figure 5.2: Image data writing control**

| MV | MX | MY | CASET                                   | PASET                                   |
|----|----|----|---|---|
| 0  | 0  | 0  | Direct to Physical Column Pointer       | Direct to Physical Page Pointer         |
| 0  | 0  | 1  | Direct to Physical Column Pointer       | Direct to (Y - Physical Page Pointer)   |
| 0  | 1  | 0  | Direct to (X-Physical Column Pointer)   | Direct to Physical Page Pointer         |
| 0  | 1  | 1  | Direct to (X - Physical Column Pointer) | Direct to (Y - Physical Page Pointer)   |
| 1  | 0  | 0  | Direct to Physical Page Pointer         | Direct to Physical Column Pointer       |
| 1  | 0  | 1  | Direct to (Y - Physical Page Pointer)   | Direct to Physical Column Pointer       |
| 1  | 1  | 0  | Direct to Physical Page Pointer         | Direct to (X-Physical Column Pointer)   |
| 1  | 1  | 1  | Direct to (Y - Physical Page Pointer)   | Direct to (X - Physical Column Pointer) |

**Table 5.2: CASET and PASET control for physical column/page pointers**

For each image orientation, the controls for the column and page counters apply as below:

| Condition   | Column Counter           | Page Counter           |
|---|--------------------------|------------------------|
| When RAMWR/RAMRD command is accepted.                 | Return to "Start Column" | Return to "Start Page" |
| Complete Pixel Pair Write/Read action                 | Increment by 1           | No change              |
| The Column counter value is larger than "End column." | Return to "Start Column" | Increment by 1         |
| The Page counter value is larger than "End page".     | Return to "Start Column" | Return to "Start Page" |

**Note:** Data is always written to the Frame Memory in the same order, regardless of the Memory Write Direction set by MX, MY, MV.

**Table 5.3: Rules for updating GRAM rorder**

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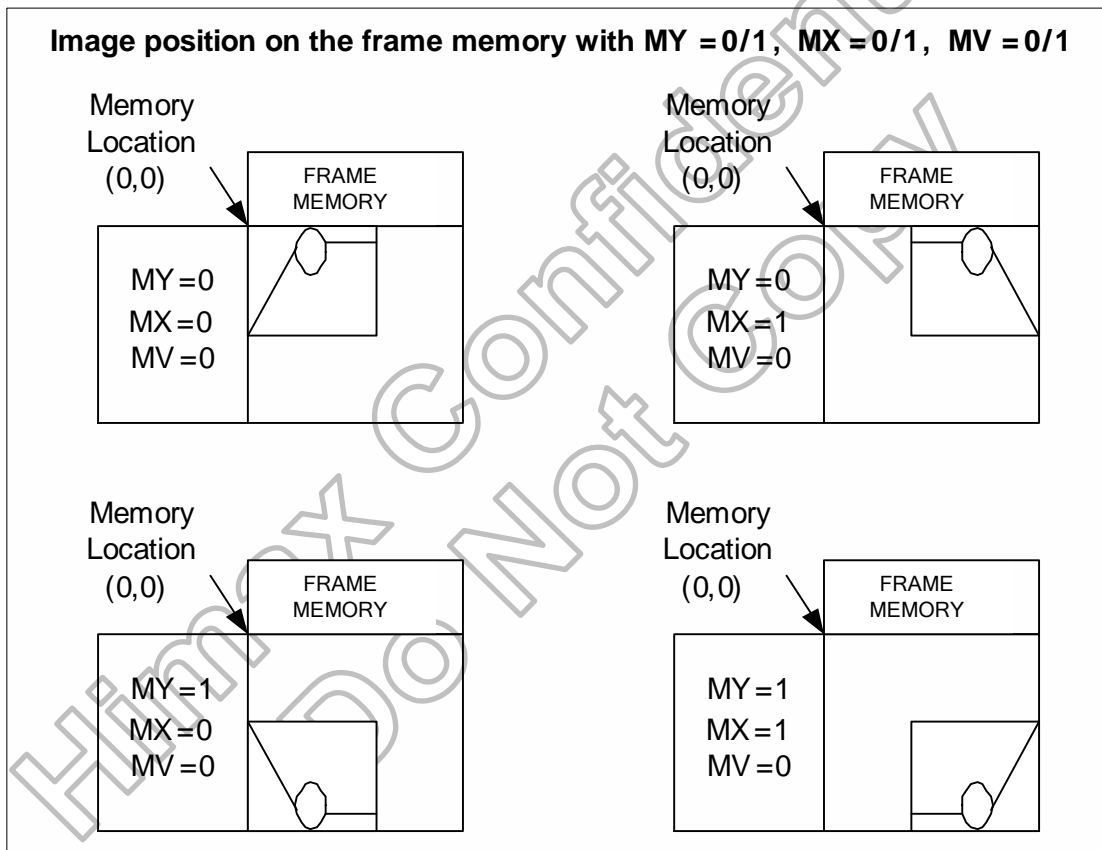
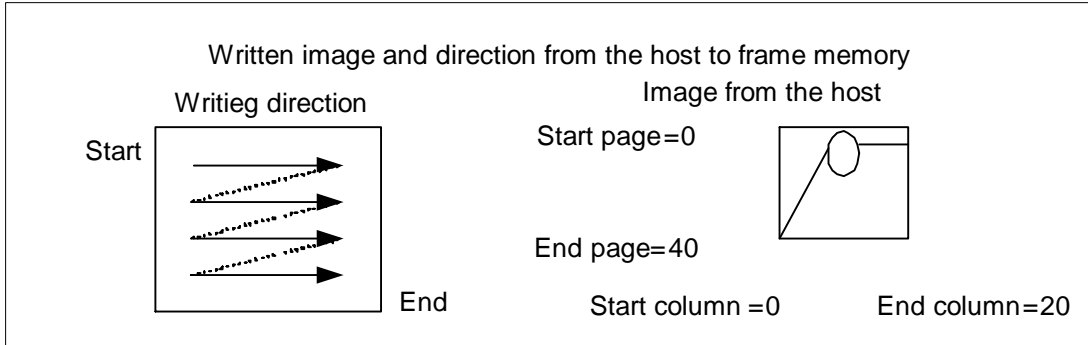
The following figure depicts the GRAM address update method with MV, MX and MY bit setting.

| Display Data Direction         | MV | MX | MY | Image in the Host | Image in the Driver (GRAM) |
|--------------------------------|----|----|----|-------------------|----------------------------|
| Normal                         | 0  | 0  | 0  |                   |                            |
| Y-Invert                       | 0  | 0  | 1  |                   |                            |
| X-Invert                       | 0  | 1  | 0  |                   |                            |
| X-Invert Y-Invert              | 0  | 1  | 1  |                   |                            |
| X-Y Exchange                   | 1  | 0  | 0  |                   |                            |
| X-Y Exchange X-invert          | 1  | 0  | 1  |                   |                            |
| X-Y Exchange Y-invert          | 1  | 1  | 0  |                   |                            |
| X-Y Exchange X-invert Y-invert | 1  | 1  | 1  |                   |                            |

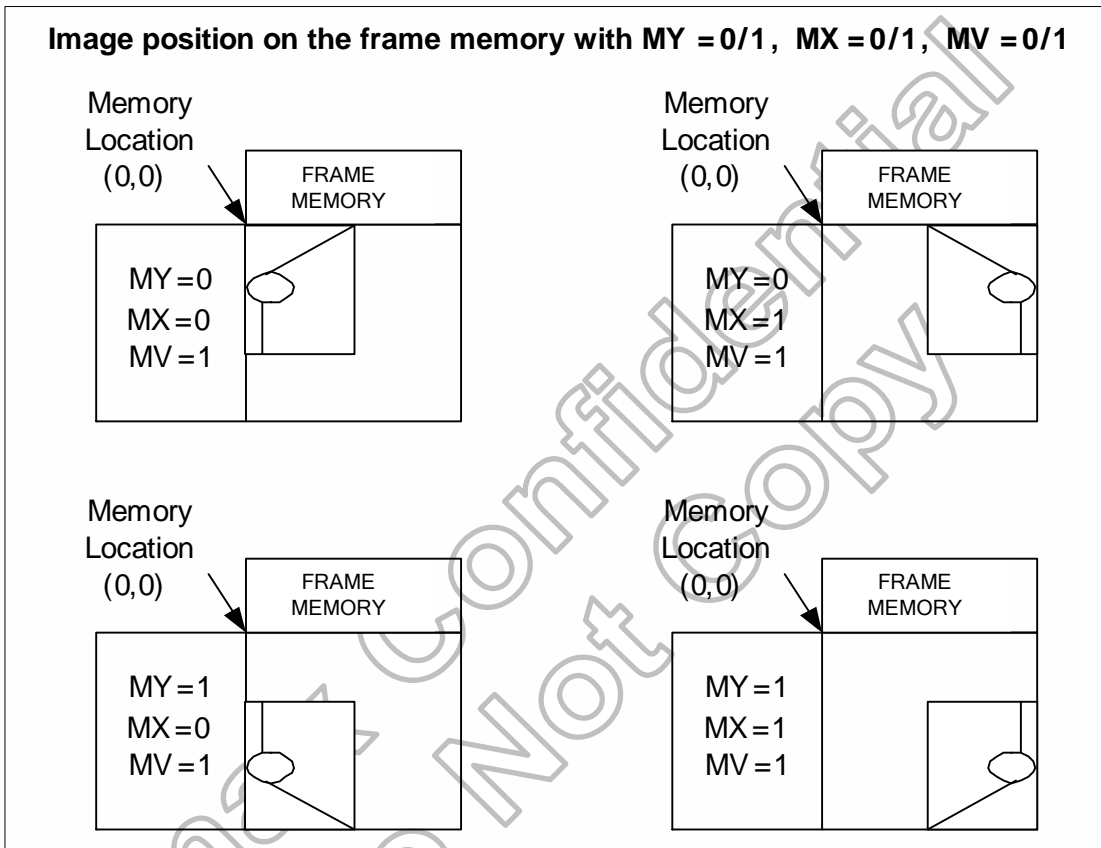
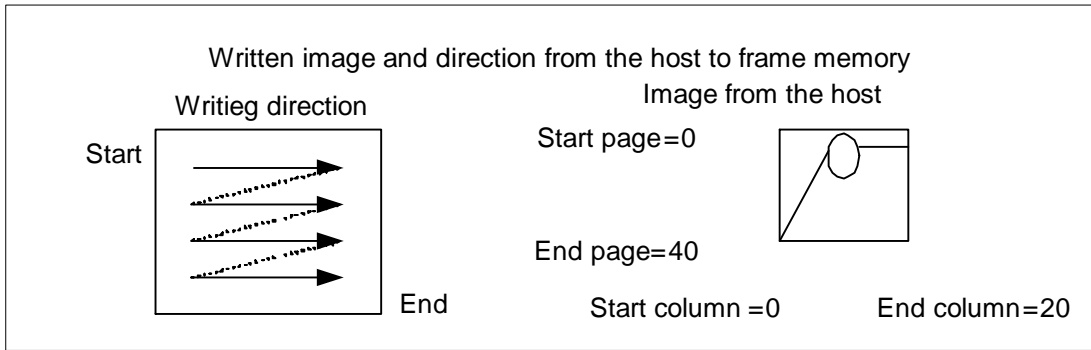
Table 5.4: Address direction settings

**Example for rotation with MY, MX and MV**

This example is using following values: start page = 0, end page = 40, start column = 0 and end column = 20 => commands: page address set (0, 40) and column address set (0, 20). The sent figure is as follows and its sending order is as follows.



**Figure 5.3: Example for rotation with MY, MX and MV - 1**



**Figure 5.4: Example for rotation with MY, MX and MV - 2**



### 5.3 GRAM to display address mapping

By setting the **SS\_Panel**, the relation between the source output channel and the GRAM address can be changed as reverse display. By setting the **GS\_Panel**, the relation between the gate output channel and the GRAM address can be changed as reverse display. By setting the **BGR\_Panel**, the relation between the source output channel and the <R>, <G>, <B> dot allocation can be reversed for different LCD color filter arrangement. Table 5.5, Table 5.6 and Table 5.7 show relations among the GRAM data allocation, the source output channel, and the R, G, B dot allocation.

| BGR_Panel = '0' |                |         |      |      |         |      |      |       |           |      |      |           |      |      |
|-----------------|----------------|---------|------|------|---------|------|------|-------|-----------|------|------|-----------|------|------|
| Source          | SS_Panel = '0' | S1      | S2   | S3   | S4      | S5   | S6   | ----- | S715      | S716 | S717 | S718      | S719 | S720 |
| Output          | SS_Panel = '1' | S718    | S719 | S720 | S715    | S716 | S717 | ----- | S4        | S5   | S6   | S1        | S2   | S3   |
| X Address       |                | "00"h   |      |      | "01"h   |      |      | ----- | "EE"h     |      |      | "EF"h     |      |      |
| RGB data        |                | R       | G    | B    | R       | G    | B    | ----- | R         | G    | B    | R         | G    | B    |
| Pixel           |                | Pixel 1 |      |      | Pixel 2 |      |      | ----- | Pixel 239 |      |      | Pixel 240 |      |      |

| BGR_Panel = '1' |                |         |      |      |         |      |      |       |           |      |      |           |      |      |
|-----------------|----------------|---------|------|------|---------|------|------|-------|-----------|------|------|-----------|------|------|
| Source          | SS_Panel = '0' | S3      | S2   | S1   | S6      | S5   | S4   | ----- | S717      | S716 | S715 | S720      | S719 | S718 |
| Output          | SS_Panel = '1' | S720    | S719 | S718 | S717    | S716 | S715 | ----- | S6        | S5   | S4   | S3        | S2   | S1   |
| X Address       |                | "00"h   |      |      | "01"h   |      |      | ----- | "EE"h     |      |      | "EF"h     |      |      |
| Bit Allocation  |                | R       | G    | B    | R       | G    | B    | ----- | R         | G    | B    | R         | G    | B    |
| Pixel           |                | Pixel 1 |      |      | Pixel 2 |      |      | ----- | Pixel 239 |      |      | Pixel 240 |      |      |

Table 5.5: GRAM X address and display panel position

| S/G pins | S1     | S2 | S3 | S4     | S5 | S6 | S7 | S8     | S9 | ----- | S709   | S710 | S711 | S712   | S713 | S714 | S715   | S716 | S717 | S718   | S719 | S720 |
|----------|--------|----|----|--------|----|----|----|--------|----|-------|--------|------|------|--------|------|------|--------|------|------|--------|------|------|
| G1       | 0000h  |    |    | 0001h  |    |    |    | 0002h  |    | ----- | 00ECh  |      |      | 00EDh  |      |      | 00EEh  |      |      | 00EFh  |      |      |
| G2       | 0100h  |    |    | 0101h  |    |    |    | 0102h  |    | ----- | 01ECh  |      |      | 01EDh  |      |      | 01EEh  |      |      | 01EFh  |      |      |
| G3       | 0200h  |    |    | 0201h  |    |    |    | 0202h  |    | ----- | 02ECh  |      |      | 02EDh  |      |      | 02EEh  |      |      | 02EFh  |      |      |
| G4       | 0300h  |    |    | 0301h  |    |    |    | 0302h  |    | ----- | 03ECh  |      |      | 03EDh  |      |      | 03EEh  |      |      | 03EFh  |      |      |
| G5       | 0400h  |    |    | 0401h  |    |    |    | 0402h  |    | ----- | 04ECh  |      |      | 04EDh  |      |      | 04EEh  |      |      | 04EFh  |      |      |
| G6       | 0500h  |    |    | 0501h  |    |    |    | 0502h  |    | ----- | 05ECh  |      |      | 05EDh  |      |      | 05EEh  |      |      | 05EFh  |      |      |
| G7       | 0600h  |    |    | 0601h  |    |    |    | 0602h  |    | ----- | 06ECh  |      |      | 06EDh  |      |      | 06EEh  |      |      | 06EFh  |      |      |
| G8       | 0700h  |    |    | 0701h  |    |    |    | 0702h  |    | ----- | 07ECh  |      |      | 07EDh  |      |      | 07EEh  |      |      | 07EFh  |      |      |
| G9       | 0800h  |    |    | 0801h  |    |    |    | 0802h  |    | ----- | 08ECh  |      |      | 08EDh  |      |      | 08EEh  |      |      | 08EFh  |      |      |
| ---      | ---    |    |    | ---    |    |    |    | ---    |    | ----- | ---    |      |      | ---    |      |      | ---    |      |      | ---    |      |      |
| G311     | 13600h |    |    | 13601h |    |    |    | 13602h |    | ----- | 136ECh |      |      | 136EDh |      |      | 136EEh |      |      | 136EFh |      |      |
| G312     | 13700h |    |    | 13701h |    |    |    | 13702h |    | ----- | 137ECh |      |      | 137EDh |      |      | 137EEh |      |      | 137EFh |      |      |
| G313     | 13800h |    |    | 13801h |    |    |    | 13802h |    | ----- | 138ECh |      |      | 138EDh |      |      | 138EEh |      |      | 138EFh |      |      |
| G314     | 13900h |    |    | 13901h |    |    |    | 13902h |    | ----- | 139ECh |      |      | 139EDh |      |      | 139EEh |      |      | 139EFh |      |      |
| G315     | 13A00h |    |    | 13A01h |    |    |    | 13A02h |    | ----- | 13AECh |      |      | 13AEDh |      |      | 13AEEh |      |      | 13AEFh |      |      |
| G316     | 13B00h |    |    | 13B01h |    |    |    | 13B02h |    | ----- | 13BECh |      |      | 13BEDh |      |      | 13BEEh |      |      | 13BEFh |      |      |
| G317     | 13C00h |    |    | 13C01h |    |    |    | 13C02h |    | ----- | 13CECh |      |      | 13CEDh |      |      | 13CEEh |      |      | 13CEFh |      |      |
| G318     | 13D00h |    |    | 13D01h |    |    |    | 13D02h |    | ----- | 13DECh |      |      | 13DEDh |      |      | 13DEEh |      |      | 13DEFh |      |      |
| G319     | 13E00h |    |    | 13E01h |    |    |    | 13E02h |    | ----- | 13EECh |      |      | 13EEDh |      |      | 13EEEh |      |      | 13EEFh |      |      |
| G320     | 13F00h |    |    | 13F01h |    |    |    | 13F02h |    | ----- | 13FECh |      |      | 13FEDh |      |      | 13FEEh |      |      | 13FEFh |      |      |

Table 5.6: GRAM address and display panel position (GS\_Panel = '0')

| S/G pins | S1     | S2 | S3 | S4     | S5 | S6 | S7 | S8     | S9 | ----- | S709   | S710 | S711 | S712   | S713 | S714 | S715   | S716 | S717 | S718   | S719 | S720 |
|----------|--------|----|----|--------|----|----|----|--------|----|-------|--------|------|------|--------|------|------|--------|------|------|--------|------|------|
| G320     | 0000h  |    |    | 0001h  |    |    |    | 0002h  |    | ----- | 00ECh  |      |      | 00EDh  |      |      | 00EEh  |      |      | 00EFh  |      |      |
| G319     | 0100h  |    |    | 0101h  |    |    |    | 0102h  |    | ----- | 01ECh  |      |      | 01EDh  |      |      | 01EEh  |      |      | 01EFh  |      |      |
| G318     | 0200h  |    |    | 0201h  |    |    |    | 0202h  |    | ----- | 02ECh  |      |      | 02EDh  |      |      | 02EEh  |      |      | 02EFh  |      |      |
| G317     | 0300h  |    |    | 0301h  |    |    |    | 0302h  |    | ----- | 03ECh  |      |      | 03EDh  |      |      | 03EEh  |      |      | 03EFh  |      |      |
| G316     | 0400h  |    |    | 0401h  |    |    |    | 0402h  |    | ----- | 04ECh  |      |      | 04EDh  |      |      | 04EEh  |      |      | 04EFh  |      |      |
| G315     | 0500h  |    |    | 0501h  |    |    |    | 0502h  |    | ----- | 05ECh  |      |      | 05EDh  |      |      | 05EEh  |      |      | 05EFh  |      |      |
| G314     | 0600h  |    |    | 0601h  |    |    |    | 0602h  |    | ----- | 06ECh  |      |      | 06EDh  |      |      | 06EEh  |      |      | 06EFh  |      |      |
| G313     | 0700h  |    |    | 0701h  |    |    |    | 0702h  |    | ----- | 07ECh  |      |      | 07EDh  |      |      | 07EEh  |      |      | 07EFh  |      |      |
| G312     | 0800h  |    |    | 0801h  |    |    |    | 0802h  |    | ----- | 08ECh  |      |      | 08EDh  |      |      | 08EEh  |      |      | 08EFh  |      |      |
| ---      | ---    |    |    | ---    |    |    |    | ---    |    | ----- | ---    |      |      | ---    |      |      | ---    |      |      | ---    |      |      |
| G10      | 13600h |    |    | 13601h |    |    |    | 13602h |    | ----- | 136ECh |      |      | 136EDh |      |      | 136EEh |      |      | 136EFh |      |      |
| G9       | 13700h |    |    | 13701h |    |    |    | 13702h |    | ----- | 137ECh |      |      | 137EDh |      |      | 137EEh |      |      | 137EFh |      |      |
| G8       | 13800h |    |    | 13801h |    |    |    | 13802h |    | ----- | 138ECh |      |      | 138EDh |      |      | 138EEh |      |      | 138EFh |      |      |
| G7       | 13900h |    |    | 13901h |    |    |    | 13902h |    | ----- | 139ECh |      |      | 139EDh |      |      | 139EEh |      |      | 139EFh |      |      |
| G6       | 13A00h |    |    | 13A01h |    |    |    | 13A02h |    | ----- | 13AECh |      |      | 13AEDh |      |      | 13AEEh |      |      | 13AEFh |      |      |
| G5       | 13B00h |    |    | 13B01h |    |    |    | 13B02h |    | ----- | 13BECh |      |      | 13BEDh |      |      | 13BEEh |      |      | 13BEFh |      |      |
| G4       | 13C00h |    |    | 13C01h |    |    |    | 13C02h |    | ----- | 13CECh |      |      | 13CEDh |      |      | 13CEEh |      |      | 13CEFh |      |      |
| G3       | 13D00h |    |    | 13D01h |    |    |    | 13D02h |    | ----- | 13DECh |      |      | 13DEDh |      |      | 13DEEh |      |      | 13DEFh |      |      |
| G2       | 13E00h |    |    | 13E01h |    |    |    | 13E02h |    | ----- | 13EECh |      |      | 13EEDh |      |      | 13EEEh |      |      | 13EEFh |      |      |
| G1       | 13F00h |    |    | 13F01h |    |    |    | 13F02h |    | ----- | 13FECh |      |      | 13FEDh |      |      | 13FEEh |      |      | 13FEFh |      |      |

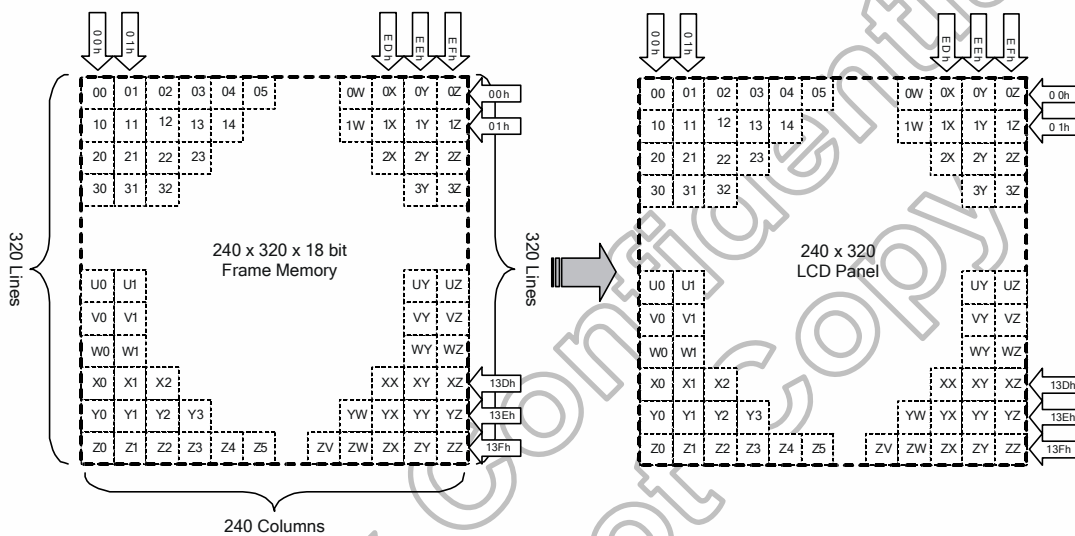
Table 5.7: GRAM address and display panel position (GS\_Panel = '0')

HX8347-G supports three kinds of display mode: one is Normal Display Mode, one is the other is Partial Display Mode, and Scrolling Display Mode.

When the **PLTON** = '0' is set, HX8347-G will be into Normal Display Mode. When the **PLTON** = '1' is set, HX8347-G will be into Partial Display Mode. When the **SCROLL\_ON** = '1' is set, HX8347-G will be into Scrolling Display Mode.

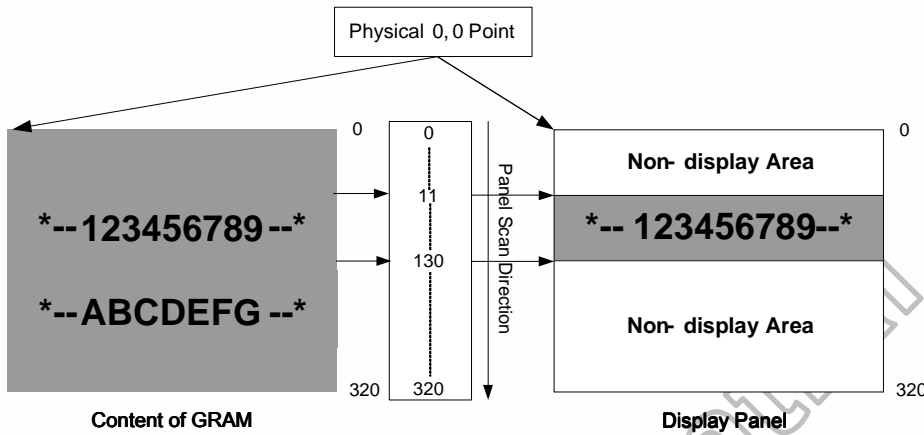
### 5.3.1 Normal display on or partial mode on, vertical scroll off

In this mode, content of the frame memory within an area where column pointer is 0000h to 00EFh and page pointer is 0000h to 013Fh is displayed. To display a dot on leftmost top corner, store the dot data at (column pointer, page pointer) = (0,0) (SS\_Panel = '0', GS\_Panel = '0').



Example:

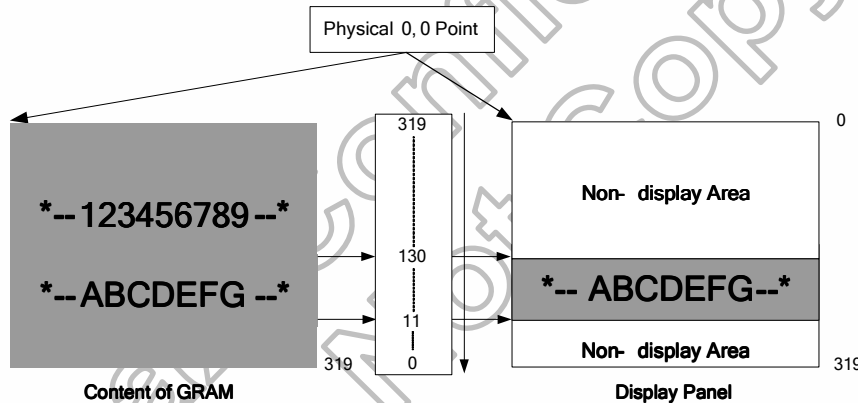
- (1) **PLTON** = '1',
- (2) **PSL** [15:0] = 11<sub>DEC</sub>, **PEL** [15:0] = 130<sub>DEC</sub>, **MADCTL**'s B4(ML)='0' (**GS\_Panel** = '0').



**Figure 5.5: Partial Display Area Setting (ML='0')**

Example:

- (1) **PLTON** = '1',
- (2) **PSL** [15:0] = 11<sub>DEC</sub>, **PEL** [15:0] = 130<sub>DEC</sub>, **MADCTL**'s B4(ML)='1' (**GS\_Panel** = '0').



**Figure 5.6: Partial Display Area Setting (ML='1')**

The refresh gate scan cycle in the rest display area of the screen (non-display area) can be specified by **ISC[3:0]** bits. The scan cycle is set to an odd number from 0~13. The polarity is inverted every scan cycle.

| ISC3 | ISC2 | ISC1 | ISC0 | Scan Cycle        | f <sub>FLM</sub> = 60Hz |
|------|------|------|------|-------------------|-------------------------|
| 0    | 0    | 0    | 0    | 1 frame           | 17ms                    |
| 0    | 0    | 0    | 1    | 5 frames          | 84ms                    |
| 0    | 0    | 1    | 0    | 9 frames          | 150ms                   |
| :    | :    | :    | :    | :                 |                         |
| 1    | 1    | 0    | 1    | 53 frames         | 880ms                   |
| 1    | 1    | 1    | 0    | 57 frames         | 946ms                   |
| 1    | 1    | 1    | 1    | Setting Inhibited | -                       |

**Table 5.8: ISC [3:0] Bits Definition**

The rest display area (non-display area) will be the white display if the type of LCD is normally white (**REV\_panel** = "0") and will be the black display if the type of LCD is normally black (**REV\_panel** = "1") in refresh gate scan cycle.

### 5.3.2 Vertical scroll display mode

When **SCROLL\_ON** bit is set to '1', the scrolling display mode is active, and the vertical scrolling display is specified by **TFA**, **VSA**, **BFA** bits (R0Eh ~R13h) and **VSP** bits (R14~R15h).

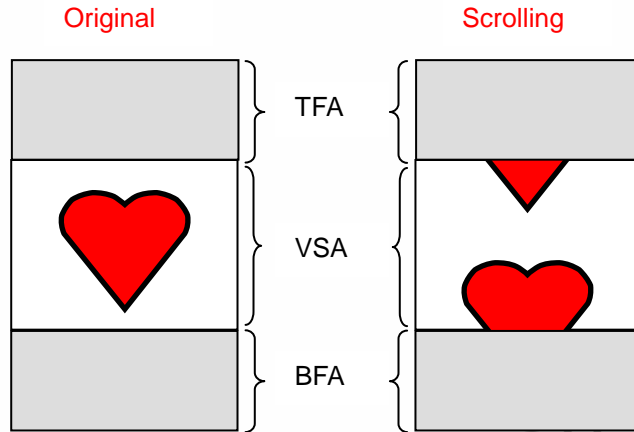


Figure 5.7: Vertical scrolling

When Vertical Scrolling Definition Parameters (TFA+VSA+BFA) = 320. In this case, scrolling is applied as shown below.

Example (1) TFA='2d', VSA='318d', BFA='0d', VSP='3d' (SS\_Panel = '0', GS\_Panel = '0')

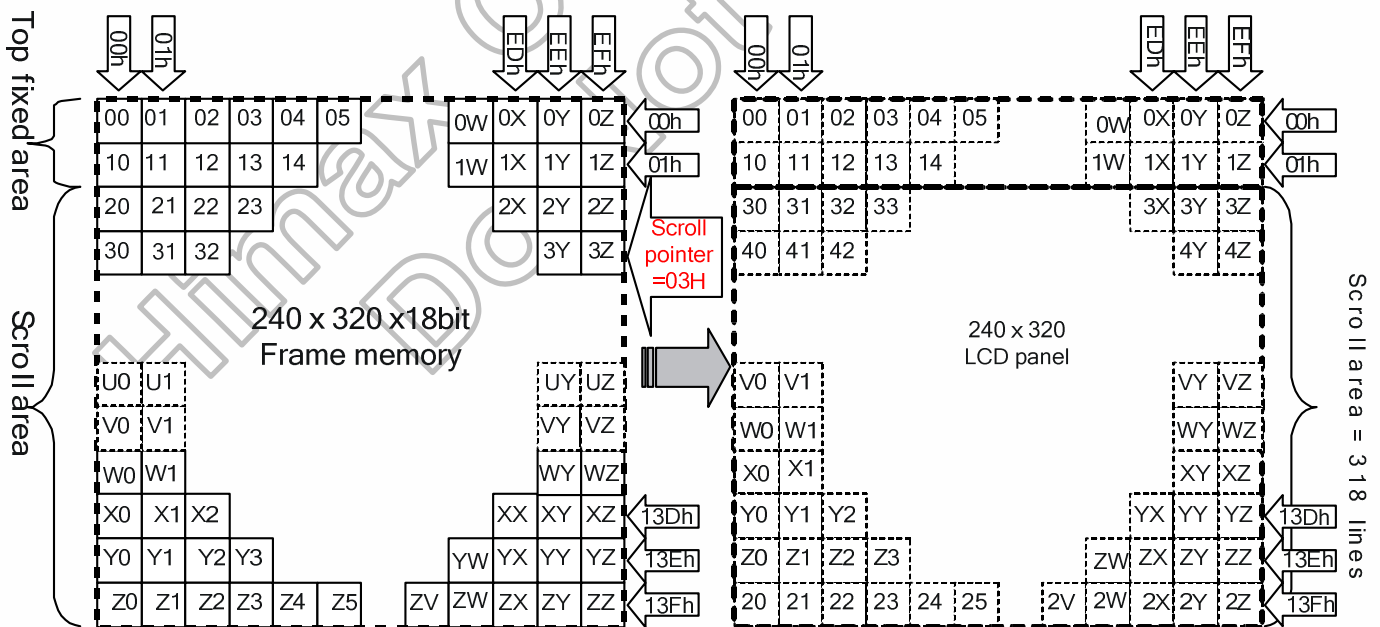


Figure 5.8: Memory map of vertical scrolling 1

Example (2) TFA='2d', VSA='316d', BFA='2d', VSP='3d' (SS\_Panel = '0', GS\_Panel = '0')

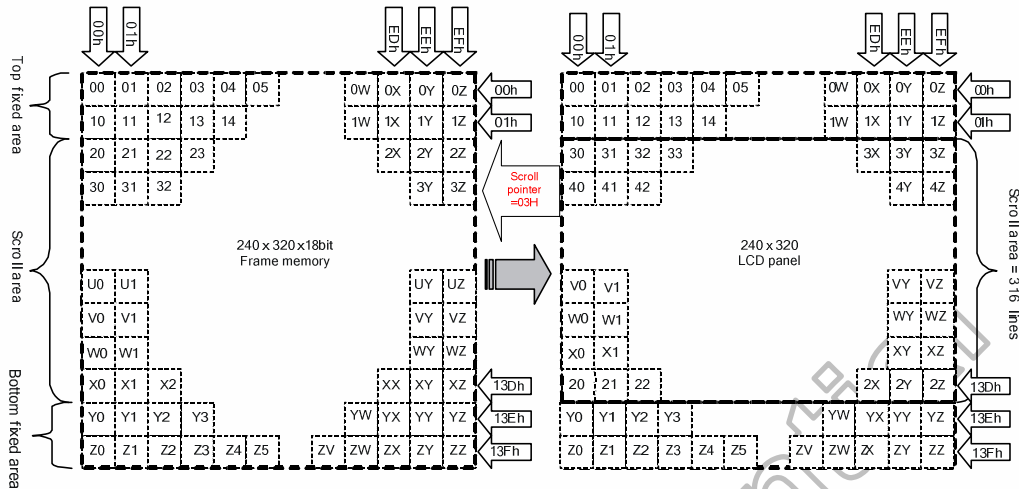


Figure 5.9: Memory map of vertical scrolling 2

Example (3) TFA='2d', VSA='316d', BFA='2d', VSP='5d' (SS\_Panel = '0', GS\_Panel = '0').

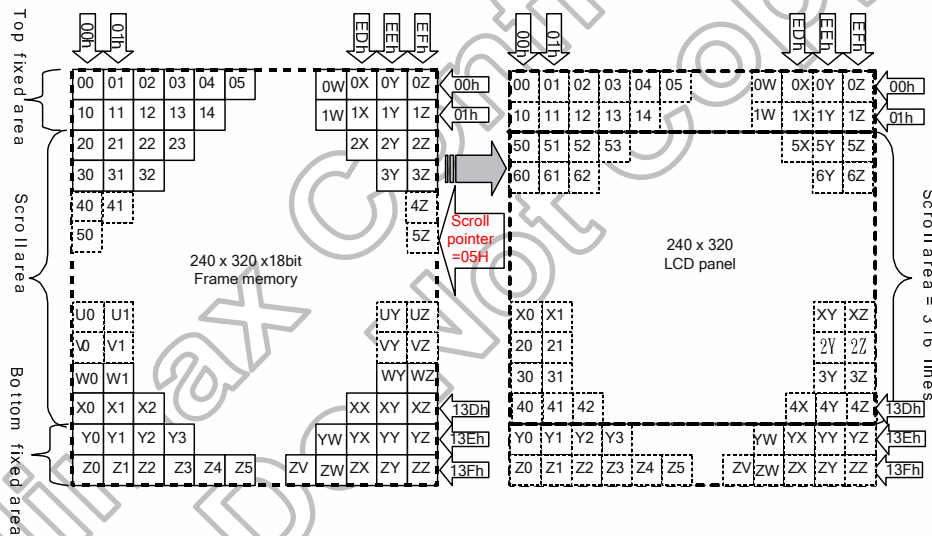


Figure 5.10: Memory map of vertical scrolling 3

**Vertical scroll example**

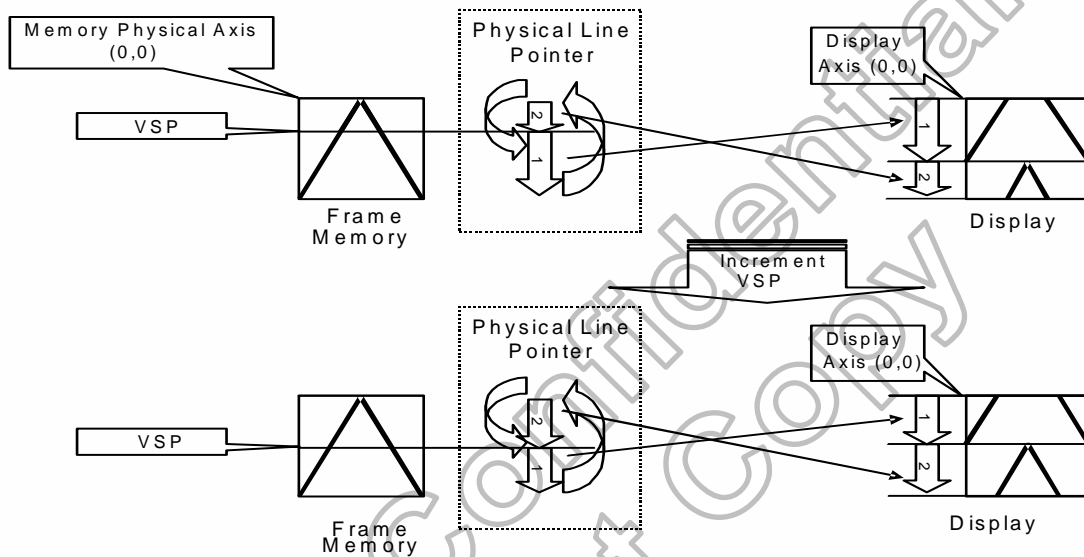
There are 2 types of vertical scrolling, which are determined by the **TFA**, **VSA**, **BFA** bits (R0Eh ~R13h) and **VSP** bits (R14~R15h).

Case 1: TFA + VSA + BFA ≠ '320d'

N/A. Do not set TFA + VSA + BFA ≠ '320d'. In that case, unexpected picture will be shown.

Case 2: TFA + VSA + BFA = '320d' (Scrolling)

Example (1) When TFA='0d', VSA='320d', BFA='0d' and VSP='40d' (SS\_Panel = '0', GS\_Panel = '0')



**Figure 5.11: Vertical scrolling example**



### 5.3.3 Updating order on display active area in RGB interface mode

There is defined different kind of updating orders for display in RGB interface mode (**RCM [1:0] = '1x'**). These updating are controlled by **MY** and **MX** bits.

Data streaming direction from the host to the display is described in the following figure.

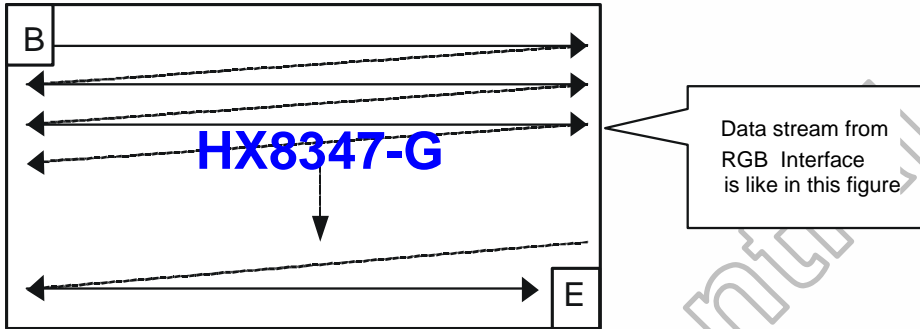


Figure 5.12: Data streaming order in RGB I/F

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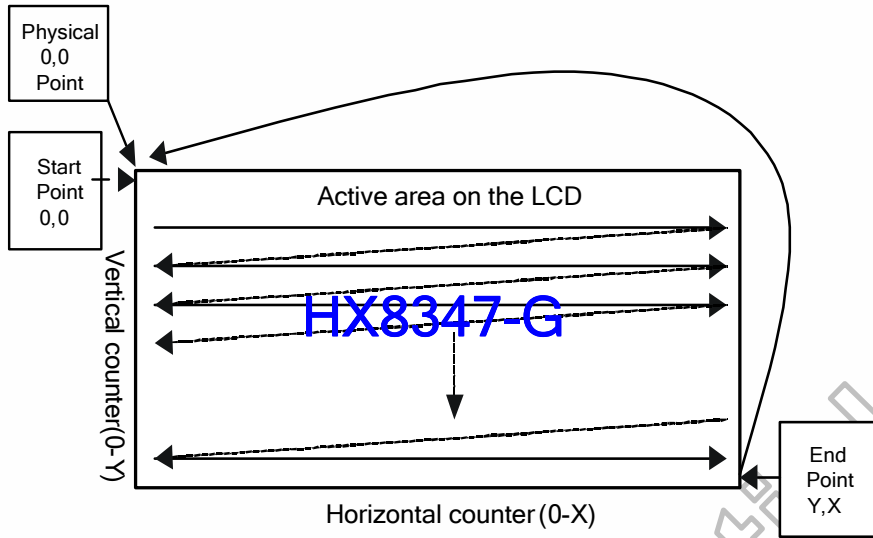


Figure 5.13: Updating order when MY = '0' and MX = '0'

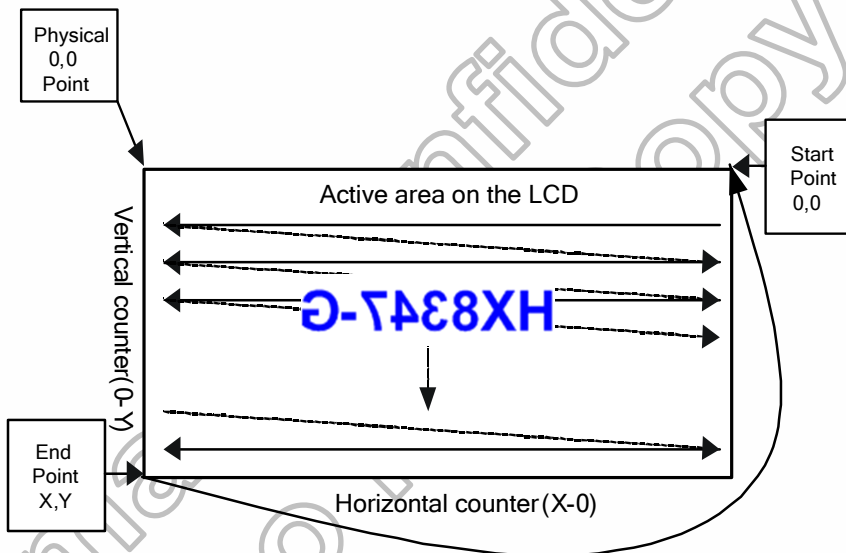


Figure 5.14: Updating order when MY = '0' and MX = '1'

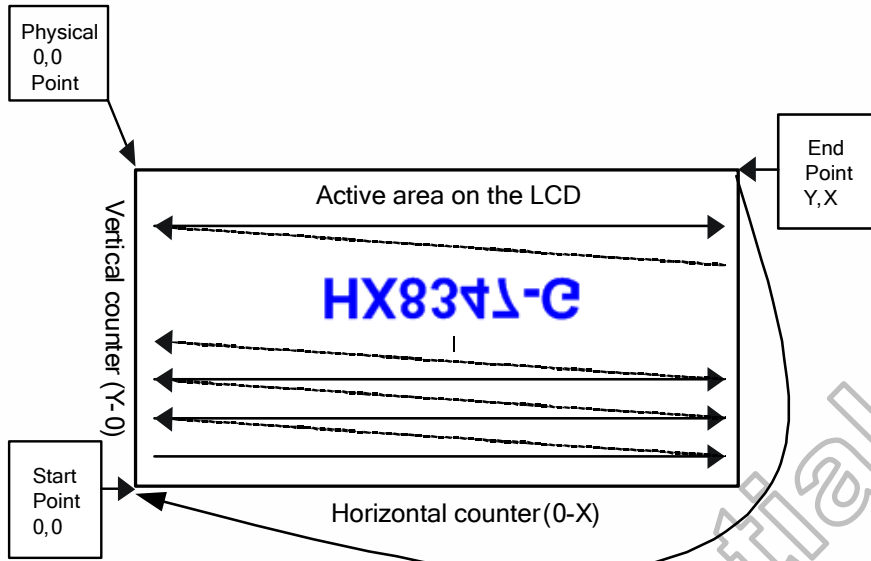


Figure 5.15: Updating order when MY = '1' and MX = '0'

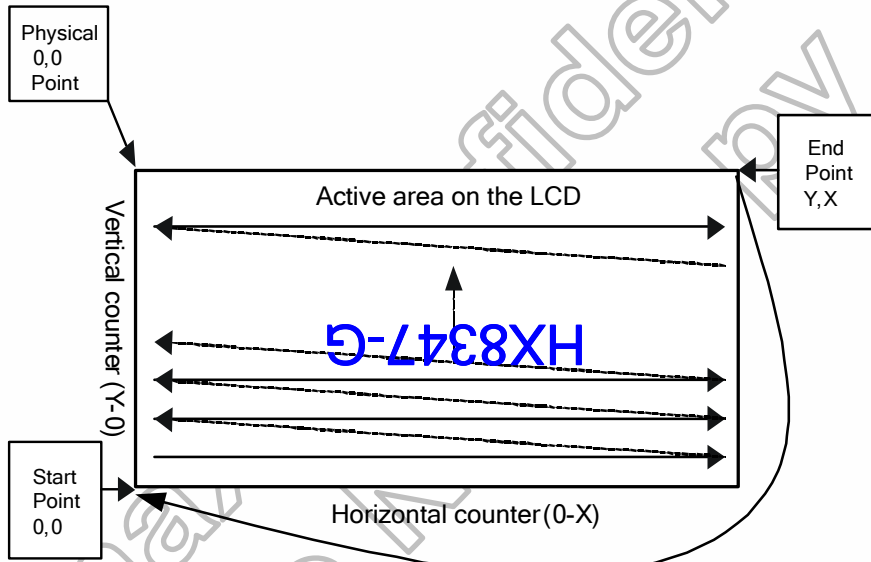


Figure 5.16: Updating order when MY = '1' and MX = '1'

| Condition   | Horizontal Counter       | Vertical Counter       |
|---|--------------------------|------------------------|
| An active VS signal is received   | Return to 0              | Return to 0            |
| Single Pixel information of the active area is received                                       | Increment by 1           | No change              |
| An active HS signal between two active area lines   | Return to 0              | Increment by 1         |
| The Horizontal counter value is larger than X and the Vertical counter value is larger than Y | Return to "Start Column" | Return to "Start Page" |

Note: Pixel order is RGB on the display.

Table 5.9: Rules for updating order on display active area in RGB interface display mode

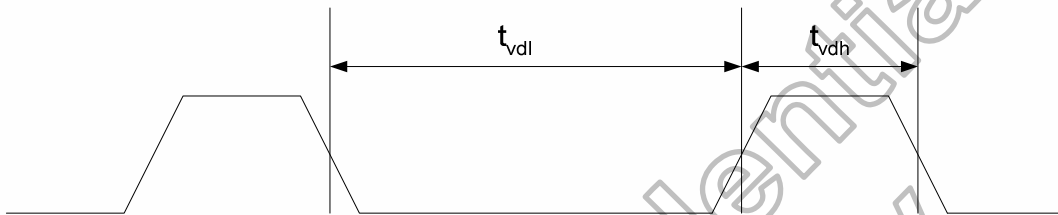
### 5.4 Tearing effect output line

The Tearing Effect output line supplies to the MPU a Panel synchronization signal. This signal can be enabled or disabled by the Tearing Effect Line Off & On commands. The mode of the Tearing Effect signal is defined by the parameter of the Tearing Effect Line On command. The signal can be used by the MPU to synchronize Frame Memory Writing when displaying video images.

Tearing effect function is not supported for RGB interface (RCM[1:0]="1x").

#### 5.4.1 Tearing effect line modes

**Mode 1**, The Tearing Effect Output signal consists of V-Blanking Information only:



$t_{vdh}$  = The LCD display is not updated from the Frame Memory

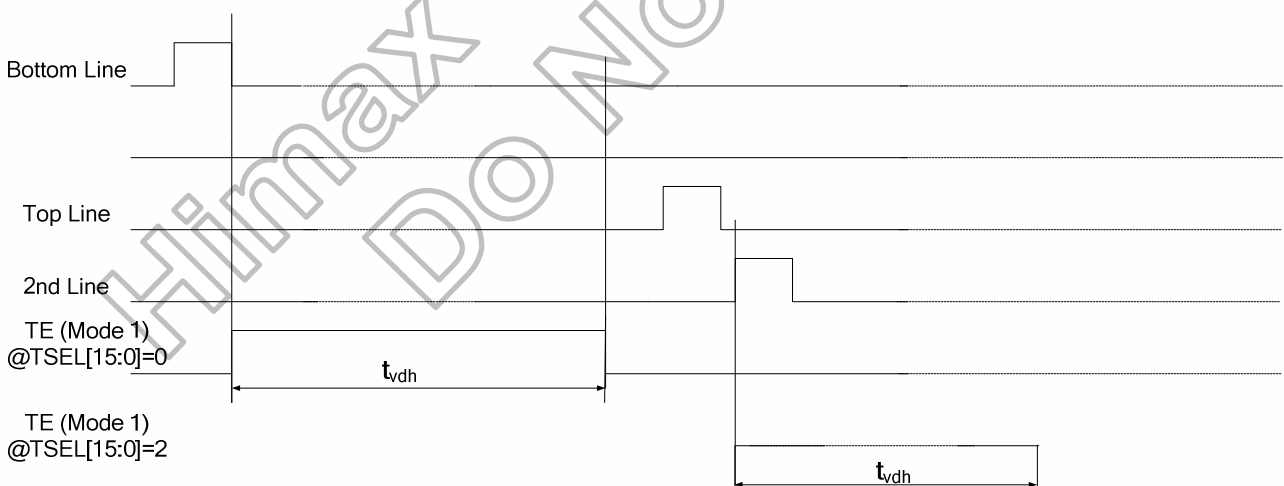
$t_{vdl}$  = The LCD display is updated from the Frame Memory (except Invisible Line – see below)

**Figure 5.17: TE mode 1 output**

Under Mode1, the TE output timing will be defined by TSEL[15:0] setting.

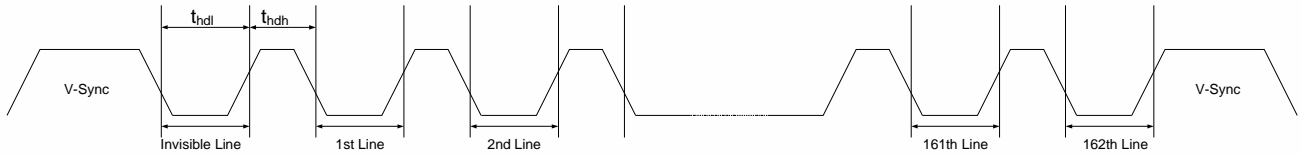
Ex:

1. TSEL[15:0]=0, then TE signal will output after last Line finished.
2. TSEL[15:0]=2, then TE signal will output at second Line start.



**Figure 5.18: TE delay output**

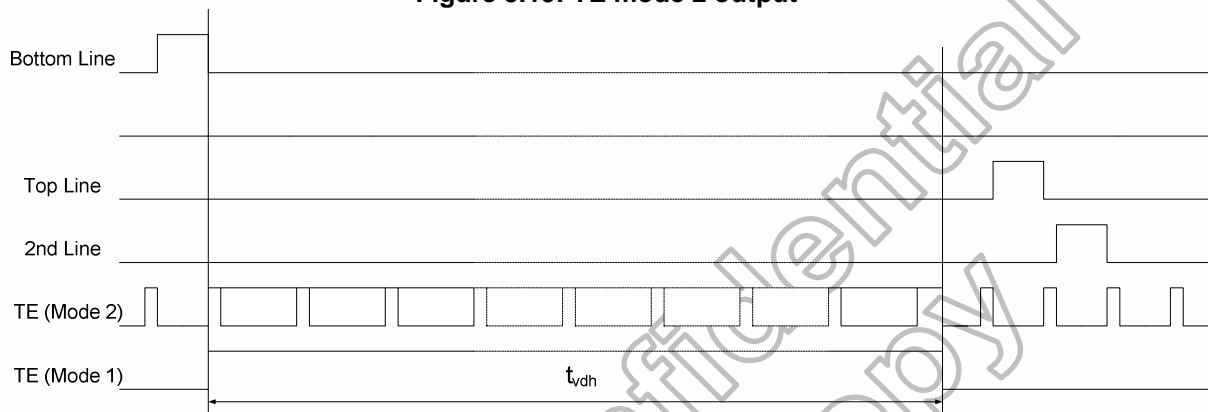
**Mode 2**, The Tearing Effect Output signal consists of V-Blanking and H-Blanking Information, there is one V-sync and 320 H-sync pulses per field.



$t_{hdh}$  = The LCD display is not updated from the Frame Memory

$t_{hdl}$  = The LCD display is updated from the Frame Memory (except Invisible Line – see above)

**Figure 5.19: TE mode 2 output**

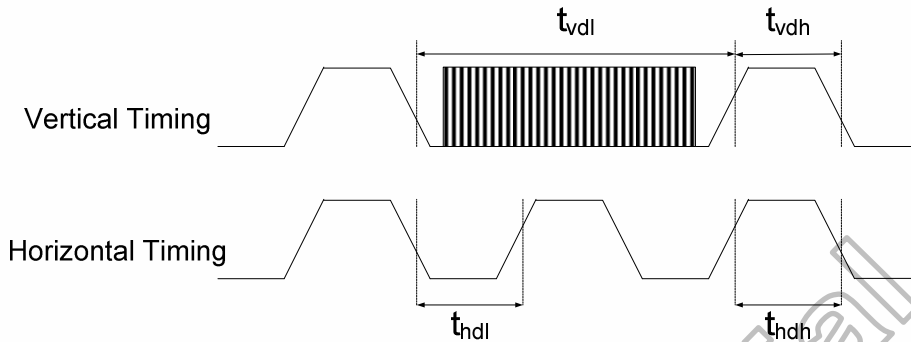


**Note:** During Sleep in Mode, the Tearing Output Pin is active Low.

**Figure 5.20: TE output waveform**

**5.4.2 Tearing effect line timing**

The Tearing Effect signal is described below.



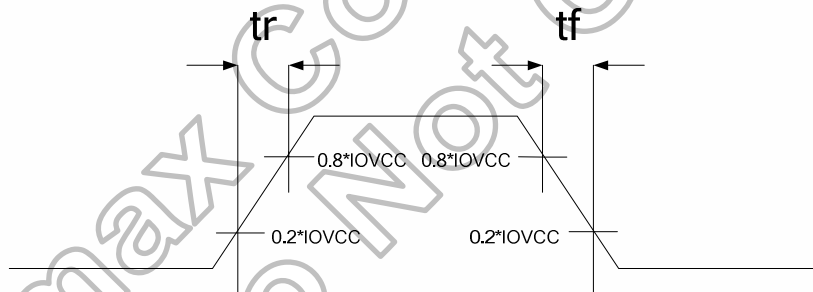
**Figure 5.21: Waveform of tearing effect signal**

Idle Mode Off (Frame Rate = 60 Hz)

| Symbol           | Parameter                       | Spec. |      |      | Description |
|------------------|---------------------------------|-------|------|------|-------------|
|                  |                                 | Min.  | Max. | Unit |             |
| t <sub>vdl</sub> | Vertical Timing Low Duration    | TBD   | -    | ms   | -           |
| t <sub>vdh</sub> | Vertical Timing High Duration   | 1000  | -    | μs   | -           |
| t <sub>hdl</sub> | Horizontal Timing Low Duration  | TBD   | -    | μs   | -           |
| t <sub>hdh</sub> | Horizontal Timing High Duration | TBD   | 500  | μs   | -           |

**Note:** The signal's rise and fall times (t<sub>f</sub>, t<sub>r</sub>) are stipulated to be equal to or less than 15ns.

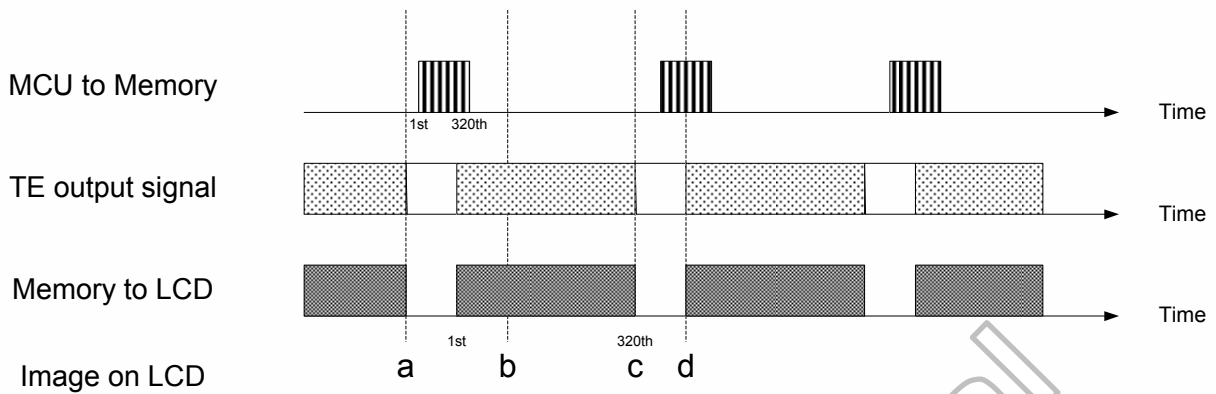
**Table 5.10: AC characteristics of tearing effect signal**



**Figure 5.22: Timing of tearing effect signal**

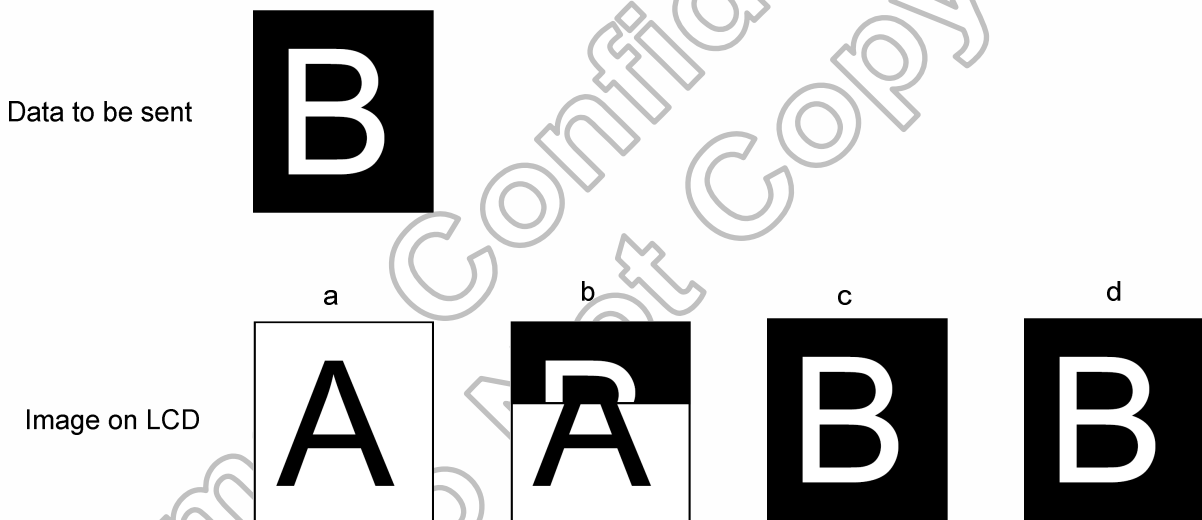
The Tearing Effect Output Line is fed back to the MPU and should be used as shown below to avoid Tearing Effect:

**5.4.3 Example 1: MPU write is faster than panel read**



**Figure 5.23: Timing of MPU write is faster than panel read**

Data write to Frame Memory is now synchronized to the Panel Scan. It should be written during the vertical sync pulse of the Tearing Effect Output Line. This ensures that data is always written ahead of the panel scan and each Panel Frame refresh has a complete new image.



**Figure 5.24: Display of MPU write is faster than panel read**



### 5.4.4 Example 2: MPU write is slower than panel read

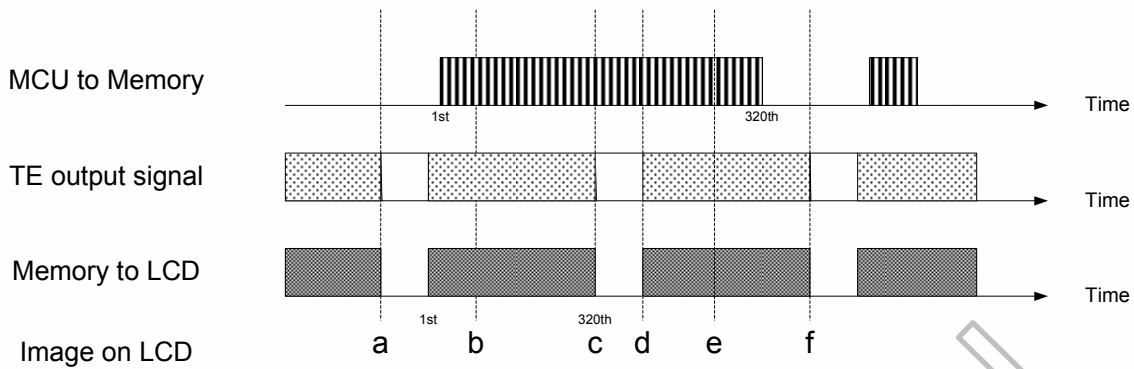


Figure 5.25: Timing of MPU write is slower than panel read

The MPU to Frame Memory write begins just after Panel Read has commenced i.e. after one horizontal sync pulse of the Tearing Effect Output Line. This allows time for the image to download behind the Panel Read pointer and finishing download during the subsequent Frame before the Read Pointer “catches” the MPU to Frame memory write position.

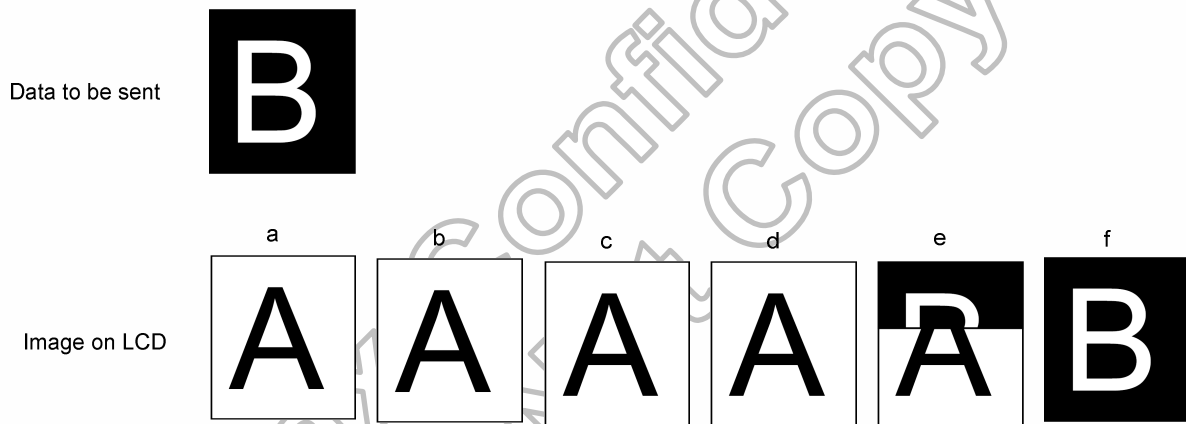


Figure 5.26: Display of MPU write is slower than panel read

### 5.5 Oscillator

The HX8347-G can oscillate an internal R-C oscillator for internal operation. Because the tolerance of internal oscillator frequency is  $\pm 5\%$ , **RADJ [3:0]** bits for initial **2.75MHz** internal clock generation. With other dividers setting, the **2.75MHz** internal clock can be used to generate clock for other part of the chip using.

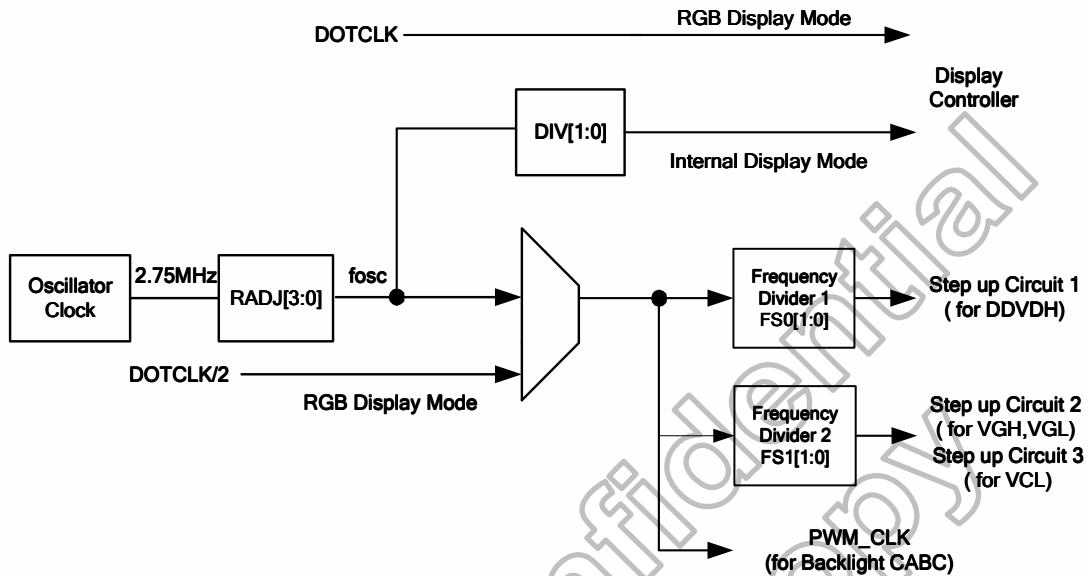


Figure 5.27: HX8347-G internal clock circuit

### 5.6 Source driver

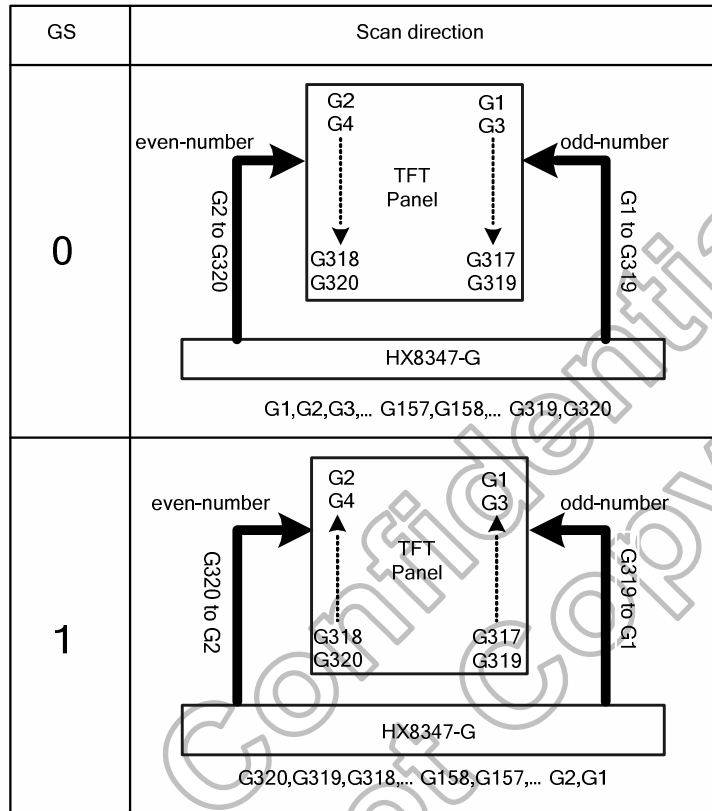
The HX8347-G contains a 720 channels of source driver (S1~S720) which is used for driving the source line of TFT LCD panel. The source driver converts the digital data from GRAM into the analog voltage for 720 channels and generates corresponding gray scale voltage output, which can realize a 262K colors display simultaneously. Since the output circuit of this source driver incorporates an operational amplifier, a positive and a negative voltage can be alternately outputted from each channel.

### 5.7 Gate driver

The HX8347-G contains a 320 gate channels of gate driver (G1~G320) which is used for driving the gate. The gate driver level is VGH when scan some line, VGL the other lines.

**5.8 Scan mode setting**

HX8347-G can set internal register GS\_PANEL bit to determine the pin assignment of gate. The GS\_PANEL setting allows changing the shift direction of gate outputs by connecting LCD panel with the HX8347-G.



**Figure 5.28: Gate scan mode**

## 5.9 LCD power generation circuit

### 5.9.1 Power supply circuit

The power circuit of HX8347-G is used to generate supply voltages for LCD panel driving.

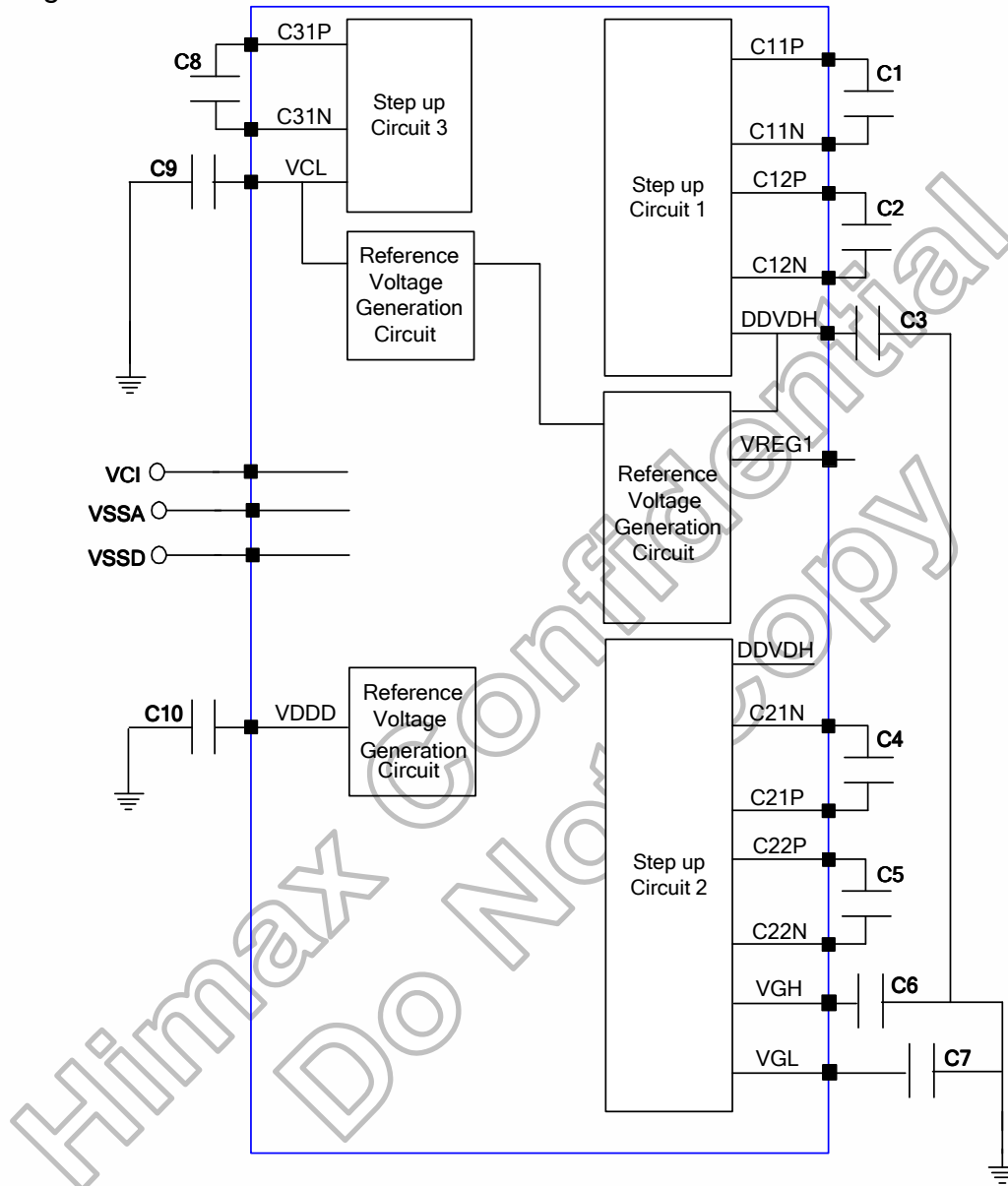


Figure 5.29: Block diagram of HX8347-G power circuit

**Specification of connected passive component**

| Capacitor   | Recommended voltage | Capacity                      |
|-------------|---------------------|-------------------------------|
| C1 (C11P/N) | 6V                  | 1 $\mu$ F (B characteristics) |
| C2 (C12P/N) | 6V                  | 1 $\mu$ F (B characteristics) |
| C3 (DDVDH)  | 10V                 | 1 $\mu$ F (B characteristics) |
| C4 (C21P/N) | 10V                 | 1 $\mu$ F (B characteristics) |
| C5 (C22P/N) | 10V                 | 1 $\mu$ F (B characteristics) |
| C6 (VGH)    | 25V                 | 1 $\mu$ F (B characteristics) |
| C7 (VGL)    | 16V                 | 1 $\mu$ F (B characteristics) |
| C8 (C31P/N) | 6V                  | 1 $\mu$ F (B characteristics) |
| C9 (VCL)    | 6V                  | 1 $\mu$ F (B characteristics) |
| C10(VDDD)   | 6V                  | 1 $\mu$ F (B characteristics) |

**Table 5.11: Adoptability of capacitor**

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### 5.9.2 LCD power generation scheme

The boost voltage generated is shown as below.

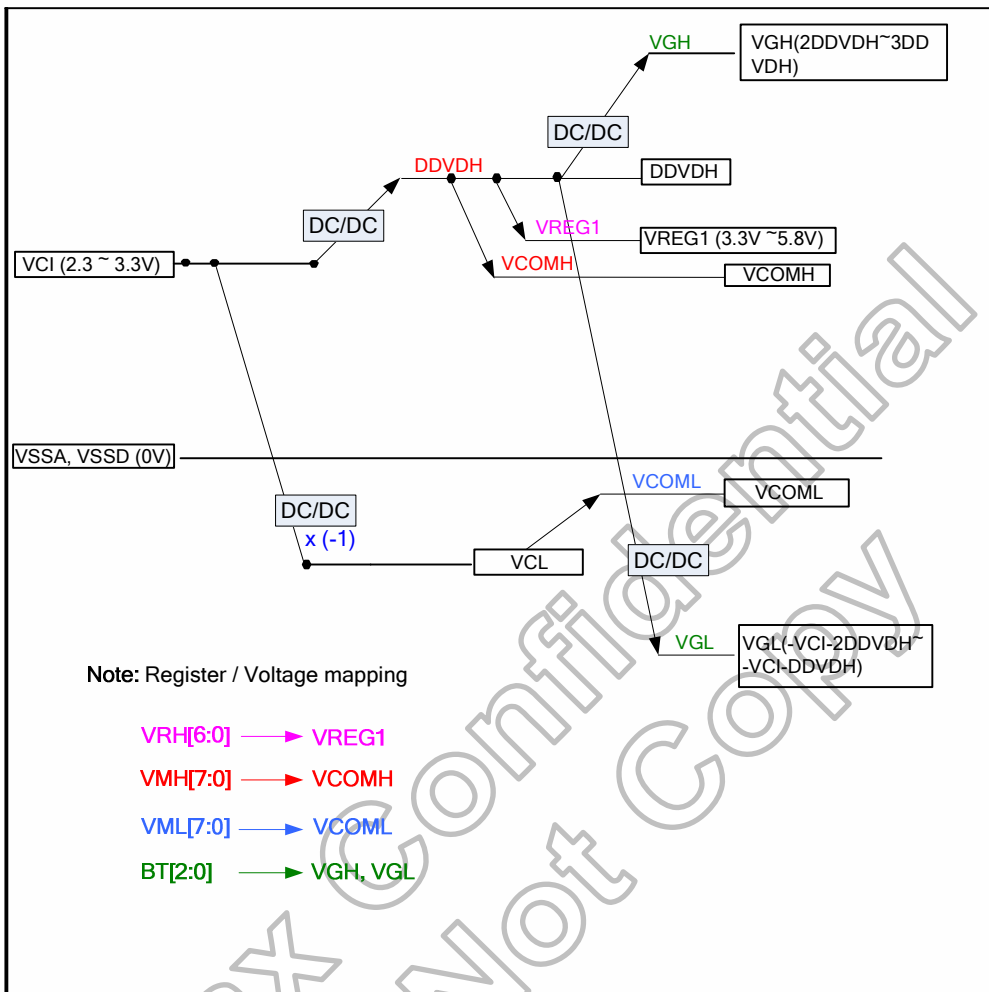
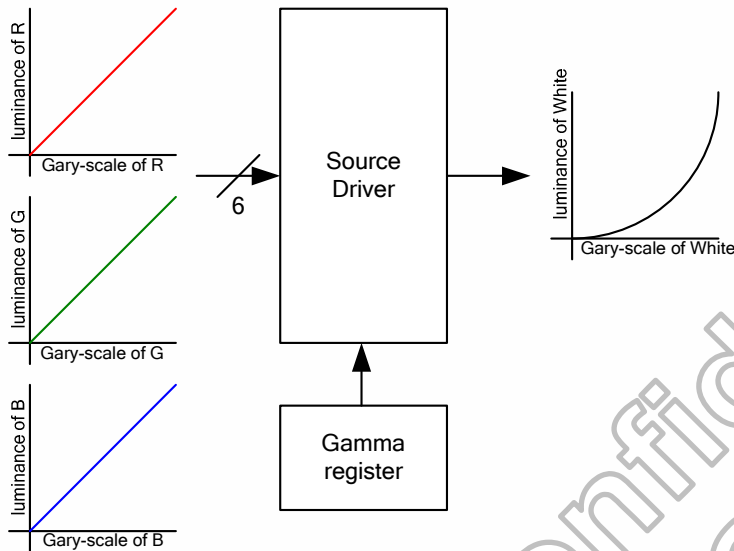


Figure 5.30: LCD power generation scheme

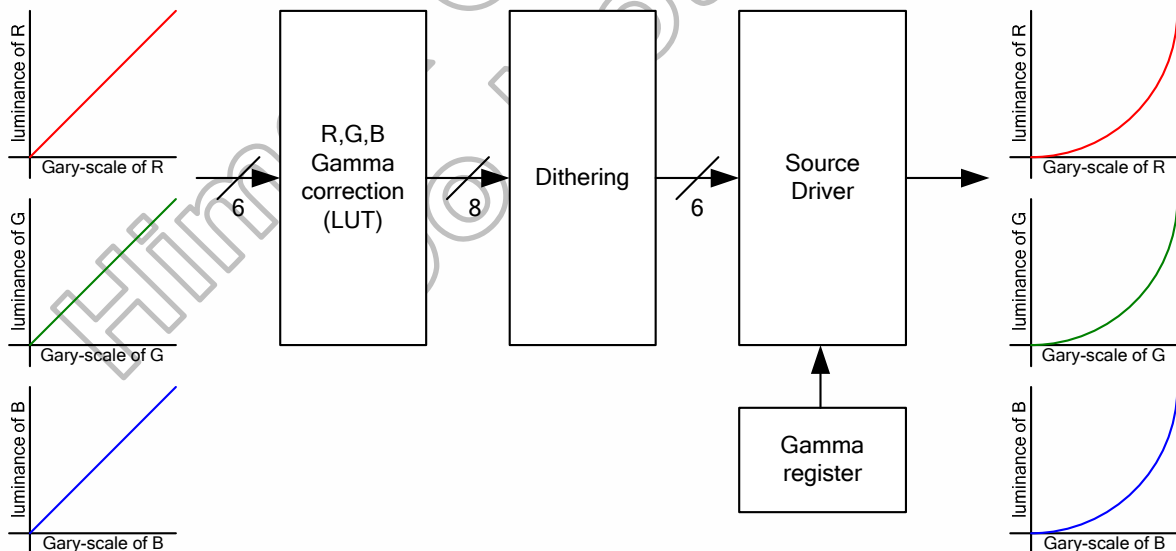
### 5.10 Gamma characteristic correction function

The HX8347-G offers two kinds of Gamma adjustment ways to come to accord with LC characteristic, one kind is through Source Driver directly, another one is adjusted by the digital gamma correction. The Gamma adjustment way is select by internal register DGC\_EN bit.

#### A) Gamma adjustment of Source Driver



#### B) Gamma adjustment of Digital Gamma Correction



**Figure 5.31: Gamma adjustments different of source driver with digital gamma correction**

The HX8347-G offers Gamma adjustment ways to come to accord with LC characteristic through Source Driver directly.



**5.10.1 Gamma characteristic correction function**

The HX8347-G incorporates gamma adjustment function for the 262,144-color display (64 grayscale for each R, G and B color). Gamma adjustment operation is implemented by deciding the 8 grayscale levels firstly in gamma adjustment control registers to match the LCD panel. These registers are available both for positive polarities and negative polarities.

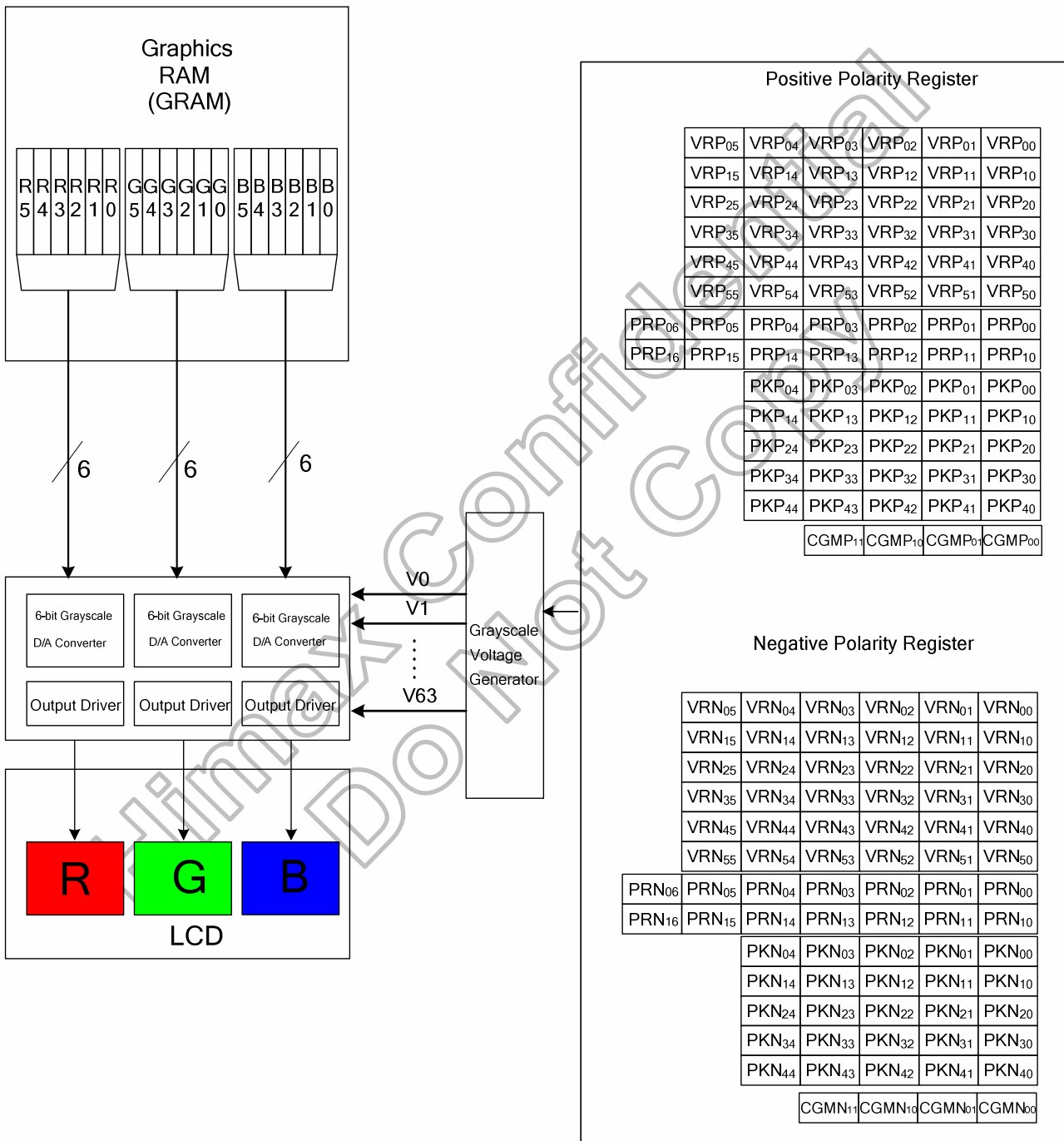


Figure 5.32: Grayscale control

**Gamma-characteristics adjustment registers**

This HX8347-G has register groups for specifying a series grayscale voltage that meets the Gamma-characteristics for the LCD panel used. These registers are divided into two groups, which correspond to the gradient, amplitude, and macro adjustment of the voltage for the grayscale characteristics. The polarity of each register can be specified independently.

**Offset adjustment registers**

The offset adjustment variable registers are used to adjust the amplitude of the grayscale voltage. This function is implemented by controlling these variable resistors in the top and bottom of the gamma resistor stream for reference gamma voltage generation. These registers are available for both positive and negative polarities

**Gamma center adjustment registers**

The gamma center adjustment registers are used to adjust the reference gamma voltage in the middle level of grayscale without changing the dynamic range. This function is implemented by choosing one input of 128-to-1 selector in the gamma resistor stream for reference gamma voltage generation. These registers are available for both positive and negative polarities.

**Gamma macro adjustment registers**

The gamma macro adjustment registers can be used for fine adjustment of the reference gamma voltage. This function is implemented by controlling the 32-to-1 selectors (PKP/N0~5), each of which has 5 inputs and generates one reference voltage output (Vg(P/N) 3, 20, 32(31), 43, 60).

| Register Groups   | Positive Polarity | Negative Polarity | Description   |
|-------------------|-------------------|-------------------|---|
| Center Adjustment | PRP0 6-0          | PRN0 6-0          | Variable resistor (PRP/N0) for center adjustment  |
|                   | PRP1 6-0          | PRN1 6-0          | Variable resistor (PRP/N1) for center adjustment  |
| Macro Adjustment  | PKP0 4-0          | PKN0 4-0          | 32-to-1 selector (voltage level of grayscale 3)   |
|                   | PKP1 4-0          | PKN1 4-0          | 32-to-1 selector (voltage level of grayscale 20)  |
|                   | PKP2 4-0          | PKN2 4-0          | 32-to-1 selector (voltage level of grayscale 32 for positive polarity and grayscale 31 for negative polarity) |
|                   | PKP3 4-0          | PKN3 4-0          | 32-to-1 selector (voltage level of grayscale 43)  |
|                   | PKP4 4-0          | PKN4 4-0          | 32-to-1 selector (voltage level of grayscale 60)  |
| Offset Adjustment | VRP0 5-0          | VRN0 5-0          | Variable resistor (VRP/N0) for offset adjustment  |
|                   | VRP1 5-0          | VRN1 5-0          | Variable resistor (VRP/N1) for offset adjustment  |
|                   | VRP2 5-0          | VRN2 5-0          | Variable resistor (VRP/N2) for offset adjustment  |
|                   | VRP3 5-0          | VRN3 5-0          | Variable resistor (VRP/N3) for offset adjustment  |
|                   | VRP4 5-0          | VRN4 5-0          | Variable resistor (VRP/N4) for offset adjustment  |
|                   | VRP5 5-0          | VRN5 5-0          | Variable resistor (VRP/N5) for offset adjustment  |

**Table 5.12: Gamma-adjustment registers**

Gamma resistor stream

The block consists of two gamma resistor streams one is for positive polarity and the other is for negative polarity, each one including eight gamma reference voltages.  $VgP/N$  (0, 1, 2, 3, 8, 20, 32(31), 43, 55, 60, 61, 62, 63). Furthermore, the block has a pin (VGS) to connect a variable resistor outside the chip for the variation between panels, if needed.

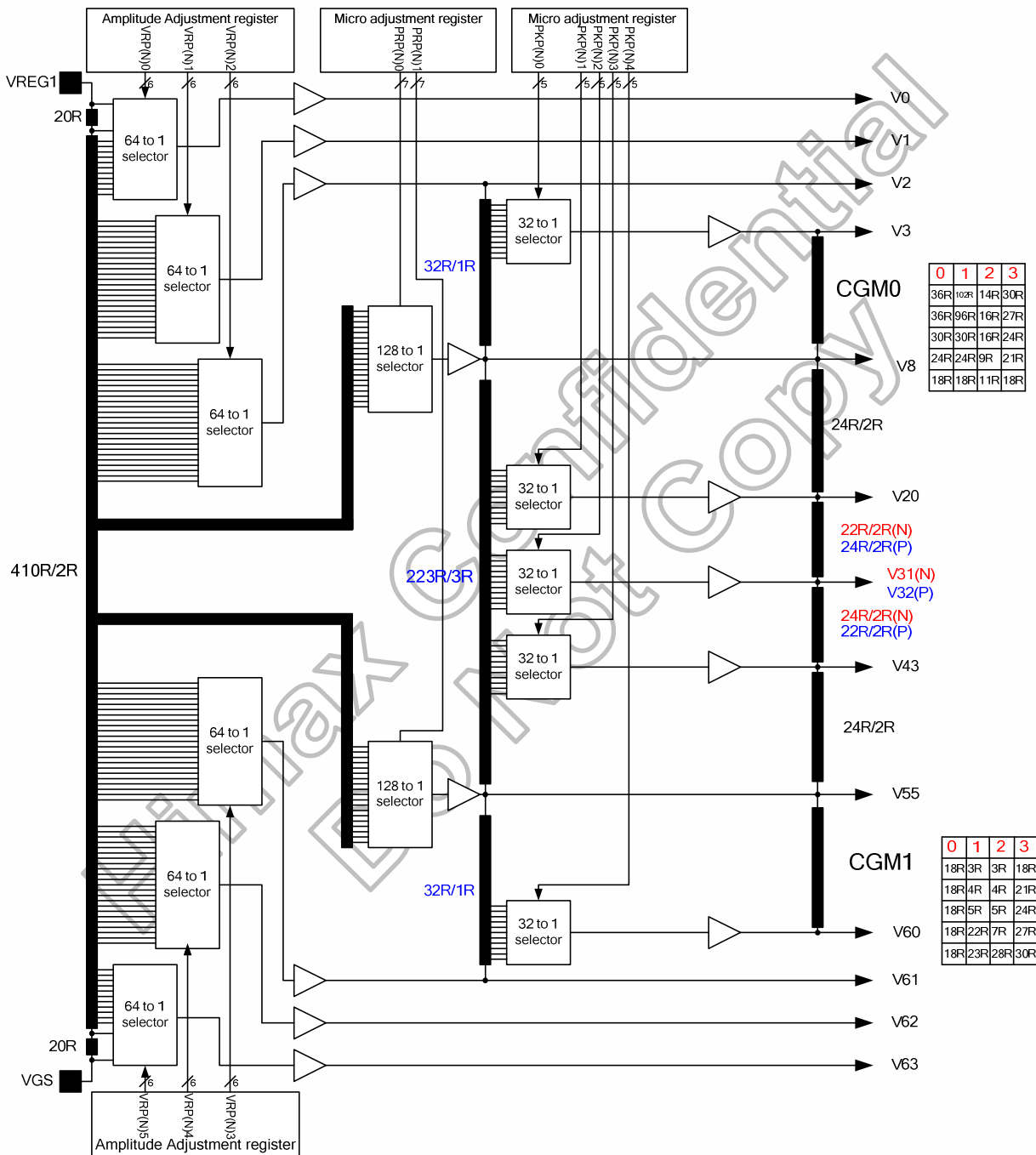


Figure 5.33: Gamma resistor stream and gamma reference voltage

**Variable resistor**

There are two types of variable resistors, one is for center adjustment and the other is for offset adjustment. The resistances are decided by setting values in the center adjustment, offset adjustment registers. Their relationships are shown below.

| Value in Register<br>VR(P/N)0 5-0 | Resistance<br>VR(P/N)0 | Value in Register<br>VR(P/N)1 5-0 | Resistance<br>VR(P/N)1 | Value in Register<br>VR(P/N)2 5-0 | Resistance<br>VR(P/N)2 |
|-----------------------------------|------------------------|-----------------------------------|------------------------|-----------------------------------|------------------------|
| 000000                            | 0R                     | 000000                            | 0R                     | 000000                            | 0R                     |
| 000001                            | 20R                    | 000001                            | 2R                     | 000001                            | 2R                     |
| 000010                            | 22R                    | 000010                            | 4R                     | 000010                            | 4R                     |
| 000011                            | 24R                    | 000011                            | 6R                     | 000011                            | 6R                     |
| •                                 | •                      | •                                 | •                      | •                                 | •                      |
| •                                 | •                      | •                                 | •                      | •                                 | •                      |
| 011101                            | 76R                    | 011101                            | 58R                    | 011101                            | 58R                    |
| 011110                            | 78R                    | 011110                            | 60R                    | 011110                            | 60R                    |
| 011111                            | 80R                    | 011111                            | 62R                    | 011111                            | 62R                    |
| 100000                            | 84R                    | 100000                            | 66R                    | 100000                            | 66R                    |
| 100001                            | 88R                    | 100001                            | 70R                    | 100001                            | 70R                    |
| 100010                            | 92R                    | 100010                            | 74R                    | 100010                            | 74R                    |
| •                                 | •                      | •                                 | •                      | •                                 | •                      |
| •                                 | •                      | •                                 | •                      | •                                 | •                      |
| 111101                            | 200R                   | 111101                            | 182R                   | 111101                            | 182R                   |
| 111110                            | 204R                   | 111110                            | 186R                   | 111110                            | 186R                   |
| 111111                            | 208R                   | 111111                            | 190R                   | 111111                            | 190R                   |

| Value in Register<br>VR(P/N)3 5-0 | Resistance<br>VR(P/N)3 | Value in Register<br>VR(P/N)4 5-0 | Resistance<br>VR(P/N)4 | Value in Register<br>VR(P/N)5 5-0 | Resistance<br>VR(P/N)2 |
|-----------------------------------|------------------------|-----------------------------------|------------------------|-----------------------------------|------------------------|
| 000000                            | 0R                     | 000000                            | 0R                     | 000000                            | 0R                     |
| 000001                            | 4R                     | 000001                            | 4R                     | 000001                            | 4R                     |
| 000010                            | 8R                     | 000010                            | 8R                     | 000010                            | 8R                     |
| •                                 | •                      | •                                 | •                      | •                                 | •                      |
| •                                 | •                      | •                                 | •                      | •                                 | •                      |
| 011101                            | 116R                   | 011101                            | 116R                   | 011101                            | 116R                   |
| 011110                            | 120R                   | 011110                            | 120R                   | 011110                            | 120R                   |
| 011111                            | 124R                   | 011111                            | 124R                   | 011111                            | 124R                   |
| 100000                            | 128R                   | 100000                            | 128R                   | 100000                            | 128R                   |
| 100001                            | 130R                   | 100001                            | 130R                   | 100001                            | 130R                   |
| 100010                            | 132R                   | 100010                            | 132R                   | 100010                            | 132R                   |
| •                                 | •                      | •                                 | •                      | •                                 | •                      |
| •                                 | •                      | •                                 | •                      | •                                 | •                      |
| 111100                            | 184R                   | 111100                            | 184R                   | 111100                            | 184R                   |
| 111101                            | 186R                   | 111101                            | 186R                   | 111101                            | 186R                   |
| 111110                            | 188R                   | 111110                            | 188R                   | 111110                            | 188R                   |
| 111111                            | 190R                   | 111111                            | 190R                   | 111111                            | 208R                   |

Table 5.13: Offset adjustment 0 ~ 5

| Value in Register<br>PR(P/N)0 6-0 | Resistance<br>PR(P/N)0 | Value in Register<br>PR(P/N)1 6-0 | Resistance<br>PR(P/N)1 |
|-----------------------------------|------------------------|-----------------------------------|------------------------|
| 0000000                           | 0R                     | 0000000                           | 0R                     |
| 0000001                           | 2R                     | 0000001                           | 2R                     |
| 0000010                           | 4R                     | 0000010                           | 4R                     |
| •                                 | •                      | •                                 | •                      |
| •                                 | •                      | •                                 | •                      |
| 1111101                           | 250R                   | 1010101                           | 250R                   |
| 1111110                           | 252R                   | 1111110                           | 252R                   |
| 1111111                           | 254R                   | 1111111                           | 254R                   |

Table 5.14: Center adjustment

The grayscale levels are determined by the following formulas:

| Reference Voltage | Macro Adjustment Value | VinP/N0 Formula                                |
|-------------------|------------------------|--|
|                   | VRP/N0 5-0 = 000000    | VREG1  |
|                   | VRP/N0 5-0 = 000001    | $((450R - 20R) / 450R) * (VREG1 - VGS) + VGS$  |
|                   | VRP/N0 5-0 = 000010    | $((450R - 22R) / 450R) * (VREG1 - VGS) + VGS$  |
|                   | VRP/N0 5-0 = 000011    | $((450R - 24R) / 450R) * (VREG1 - VGS) + VGS$  |
|                   | VRP/N0 5-0 = 000100    | $((450R - 26R) / 450R) * (VREG1 - VGS) + VGS$  |
|                   | VRP/N0 5-0 = 000101    | $((450R - 28R) / 450R) * (VREG1 - VGS) + VGS$  |
|                   | VRP/N0 5-0 = 000110    | $((450R - 30R) / 450R) * (VREG1 - VGS) + VGS$  |
|                   | VRP/N0 5-0 = 000111    | $((450R - 32R) / 450R) * (VREG1 - VGS) + VGS$  |
|                   | VRP/N0 5-0 = 001000    | $((450R - 34R) / 450R) * (VREG1 - VGS) + VGS$  |
|                   | VRP/N0 5-0 = 001001    | $((450R - 36R) / 450R) * (VREG1 - VGS) + VGS$  |
|                   | VRP/N0 5-0 = 001010    | $((450R - 38R) / 450R) * (VREG1 - VGS) + VGS$  |
|                   | VRP/N0 5-0 = 001011    | $((450R - 40R) / 450R) * (VREG1 - VGS) + VGS$  |
|                   | VRP/N0 5-0 = 001100    | $((450R - 42R) / 450R) * (VREG1 - VGS) + VGS$  |
|                   | VRP/N0 5-0 = 001101    | $((450R - 44R) / 450R) * (VREG1 - VGS) + VGS$  |
|                   | VRP/N0 5-0 = 001110    | $((450R - 46R) / 450R) * (VREG1 - VGS) + VGS$  |
|                   | VRP/N0 5-0 = 001111    | $((450R - 48R) / 450R) * (VREG1 - VGS) + VGS$  |
|                   | VRP/N0 5-0 = 010000    | $((450R - 50R) / 450R) * (VREG1 - VGS) + VGS$  |
|                   | VRP/N0 5-0 = 010001    | $((450R - 52R) / 450R) * (VREG1 - VGS) + VGS$  |
|                   | VRP/N0 5-0 = 010010    | $((450R - 54R) / 450R) * (VREG1 - VGS) + VGS$  |
|                   | VRP/N0 5-0 = 010011    | $((450R - 56R) / 450R) * (VREG1 - VGS) + VGS$  |
|                   | VRP/N0 5-0 = 010100    | $((450R - 58R) / 450R) * (VREG1 - VGS) + VGS$  |
|                   | VRP/N0 5-0 = 010101    | $((450R - 60R) / 450R) * (VREG1 - VGS) + VGS$  |
|                   | VRP/N0 5-0 = 010110    | $((450R - 62R) / 450R) * (VREG1 - VGS) + VGS$  |
|                   | VRP/N0 5-0 = 010111    | $((450R - 64R) / 450R) * (VREG1 - VGS) + VGS$  |
|                   | VRP/N0 5-0 = 011000    | $((450R - 66R) / 450R) * (VREG1 - VGS) + VGS$  |
|                   | VRP/N0 5-0 = 011001    | $((450R - 68R) / 450R) * (VREG1 - VGS) + VGS$  |
|                   | VRP/N0 5-0 = 011010    | $((450R - 70R) / 450R) * (VREG1 - VGS) + VGS$  |
|                   | VRP/N0 5-0 = 011011    | $((450R - 72R) / 450R) * (VREG1 - VGS) + VGS$  |
|                   | VRP/N0 5-0 = 011100    | $((450R - 74R) / 450R) * (VREG1 - VGS) + VGS$  |
|                   | VRP/N0 5-0 = 011101    | $((450R - 76R) / 450R) * (VREG1 - VGS) + VGS$  |
|                   | VRP/N0 5-0 = 011110    | $((450R - 78R) / 450R) * (VREG1 - VGS) + VGS$  |
|                   | VRP/N0 5-0 = 011111    | $((450R - 80R) / 450R) * (VREG1 - VGS) + VGS$  |
| VinP/N0           | VRP/N0 5-0 = 100000    | $((450R - 84R) / 450R) * (VREG1 - VGS) + VGS$  |
|                   | VRP/N0 5-0 = 100001    | $((450R - 88R) / 450R) * (VREG1 - VGS) + VGS$  |
|                   | VRP/N0 5-0 = 100010    | $((450R - 92R) / 450R) * (VREG1 - VGS) + VGS$  |
|                   | VRP/N0 5-0 = 100011    | $((450R - 96R) / 450R) * (VREG1 - VGS) + VGS$  |
|                   | VRP/N0 5-0 = 100100    | $((450R - 100R) / 450R) * (VREG1 - VGS) + VGS$ |
|                   | VRP/N0 5-0 = 100101    | $((450R - 104R) / 450R) * (VREG1 - VGS) + VGS$ |
|                   | VRP/N0 5-0 = 100110    | $((450R - 108R) / 450R) * (VREG1 - VGS) + VGS$ |
|                   | VRP/N0 5-0 = 100111    | $((450R - 112R) / 450R) * (VREG1 - VGS) + VGS$ |
|                   | VRP/N0 5-0 = 101000    | $((450R - 116R) / 450R) * (VREG1 - VGS) + VGS$ |
|                   | VRP/N0 5-0 = 101001    | $((450R - 120R) / 450R) * (VREG1 - VGS) + VGS$ |
|                   | VRP/N0 5-0 = 101010    | $((450R - 124R) / 450R) * (VREG1 - VGS) + VGS$ |
|                   | VRP/N0 5-0 = 101011    | $((450R - 128R) / 450R) * (VREG1 - VGS) + VGS$ |
|                   | VRP/N0 5-0 = 101100    | $((450R - 132R) / 450R) * (VREG1 - VGS) + VGS$ |
|                   | VRP/N0 5-0 = 101101    | $((450R - 136R) / 450R) * (VREG1 - VGS) + VGS$ |
|                   | VRP/N0 5-0 = 101110    | $((450R - 140R) / 450R) * (VREG1 - VGS) + VGS$ |
|                   | VRP/N0 5-0 = 101111    | $((450R - 144R) / 450R) * (VREG1 - VGS) + VGS$ |
|                   | VRP/N0 5-0 = 110000    | $((450R - 148R) / 450R) * (VREG1 - VGS) + VGS$ |
|                   | VRP/N0 5-0 = 110001    | $((450R - 152R) / 450R) * (VREG1 - VGS) + VGS$ |
|                   | VRP/N0 5-0 = 110010    | $((450R - 156R) / 450R) * (VREG1 - VGS) + VGS$ |
|                   | VRP/N0 5-0 = 110011    | $((450R - 160R) / 450R) * (VREG1 - VGS) + VGS$ |
|                   | VRP/N0 5-0 = 110100    | $((450R - 164R) / 450R) * (VREG1 - VGS) + VGS$ |
|                   | VRP/N0 5-0 = 110101    | $((450R - 168R) / 450R) * (VREG1 - VGS) + VGS$ |
|                   | VRP/N0 5-0 = 110110    | $((450R - 172R) / 450R) * (VREG1 - VGS) + VGS$ |
|                   | VRP/N0 5-0 = 110111    | $((450R - 176R) / 450R) * (VREG1 - VGS) + VGS$ |
|                   | VRP/N0 5-0 = 111000    | $((450R - 180R) / 450R) * (VREG1 - VGS) + VGS$ |
|                   | VRP/N0 5-0 = 111001    | $((450R - 184R) / 450R) * (VREG1 - VGS) + VGS$ |
|                   | VRP/N0 5-0 = 111010    | $((450R - 188R) / 450R) * (VREG1 - VGS) + VGS$ |
|                   | VRP/N0 5-0 = 111011    | $((450R - 192R) / 450R) * (VREG1 - VGS) + VGS$ |
|                   | VRP/N0 5-0 = 111100    | $((450R - 196R) / 450R) * (VREG1 - VGS) + VGS$ |
|                   | VRP/N0 5-0 = 111101    | $((450R - 200R) / 450R) * (VREG1 - VGS) + VGS$ |
|                   | VRP/N0 5-0 = 111110    | $((450R - 204R) / 450R) * (VREG1 - VGS) + VGS$ |
|                   | VRP/N0 5-0 = 111111    | $((450R - 208R) / 450R) * (VREG1 - VGS) + VGS$ |

Table 5.15: VinP/N 0



| Reference Voltage | Macro Adjustment Value | VinP/N1 Formula                                |
|-------------------|------------------------|--|
|                   | VRP/N1 5-0 = 000000    | $(430R / 450R) * (VREG1 - VGS) + VGS$          |
|                   | VRP/N1 5-0 = 000001    | $((430R - 2R) / 450R) * (VREG1 - VGS) + VGS$   |
|                   | VRP/N1 5-0 = 000010    | $((430R - 4R) / 450R) * (VREG1 - VGS) + VGS$   |
|                   | VRP/N1 5-0 = 000011    | $((430R - 6R) / 450R) * (VREG1 - VGS) + VGS$   |
|                   | VRP/N1 5-0 = 000100    | $((430R - 8R) / 450R) * (VREG1 - VGS) + VGS$   |
|                   | VRP/N1 5-0 = 000101    | $((430R - 10R) / 450R) * (VREG1 - VGS) + VGS$  |
|                   | VRP/N1 5-0 = 000110    | $((430R - 12R) / 450R) * (VREG1 - VGS) + VGS$  |
|                   | VRP/N1 5-0 = 000111    | $((430R - 14R) / 450R) * (VREG1 - VGS) + VGS$  |
|                   | VRP/N1 5-0 = 001000    | $((430R - 16R) / 450R) * (VREG1 - VGS) + VGS$  |
|                   | VRP/N1 5-0 = 001001    | $((430R - 18R) / 450R) * (VREG1 - VGS) + VGS$  |
|                   | VRP/N1 5-0 = 001010    | $((430R - 20R) / 450R) * (VREG1 - VGS) + VGS$  |
|                   | VRP/N1 5-0 = 001011    | $((430R - 22R) / 450R) * (VREG1 - VGS) + VGS$  |
|                   | VRP/N1 5-0 = 001100    | $((430R - 24R) / 450R) * (VREG1 - VGS) + VGS$  |
|                   | VRP/N1 5-0 = 001101    | $((430R - 26R) / 450R) * (VREG1 - VGS) + VGS$  |
|                   | VRP/N1 5-0 = 001110    | $((430R - 28R) / 450R) * (VREG1 - VGS) + VGS$  |
|                   | VRP/N1 5-0 = 001111    | $((430R - 30R) / 450R) * (VREG1 - VGS) + VGS$  |
|                   | VRP/N1 5-0 = 010000    | $((430R - 32R) / 450R) * (VREG1 - VGS) + VGS$  |
|                   | VRP/N1 5-0 = 010001    | $((430R - 34R) / 450R) * (VREG1 - VGS) + VGS$  |
|                   | VRP/N1 5-0 = 010010    | $((430R - 36R) / 450R) * (VREG1 - VGS) + VGS$  |
|                   | VRP/N1 5-0 = 010011    | $((430R - 38R) / 450R) * (VREG1 - VGS) + VGS$  |
|                   | VRP/N1 5-0 = 010100    | $((430R - 40R) / 450R) * (VREG1 - VGS) + VGS$  |
|                   | VRP/N1 5-0 = 010101    | $((430R - 42R) / 450R) * (VREG1 - VGS) + VGS$  |
|                   | VRP/N1 5-0 = 010110    | $((430R - 44R) / 450R) * (VREG1 - VGS) + VGS$  |
|                   | VRP/N1 5-0 = 010111    | $((430R - 46R) / 450R) * (VREG1 - VGS) + VGS$  |
|                   | VRP/N1 5-0 = 011000    | $((430R - 48R) / 450R) * (VREG1 - VGS) + VGS$  |
|                   | VRP/N1 5-0 = 011001    | $((430R - 50R) / 450R) * (VREG1 - VGS) + VGS$  |
|                   | VRP/N1 5-0 = 011010    | $((430R - 52R) / 450R) * (VREG1 - VGS) + VGS$  |
|                   | VRP/N1 5-0 = 011011    | $((430R - 54R) / 450R) * (VREG1 - VGS) + VGS$  |
|                   | VRP/N1 5-0 = 011100    | $((430R - 56R) / 450R) * (VREG1 - VGS) + VGS$  |
|                   | VRP/N1 5-0 = 011101    | $((430R - 58R) / 450R) * (VREG1 - VGS) + VGS$  |
|                   | VRP/N1 5-0 = 011110    | $((430R - 60R) / 450R) * (VREG1 - VGS) + VGS$  |
|                   | VRP/N1 5-0 = 011111    | $((430R - 62R) / 450R) * (VREG1 - VGS) + VGS$  |
| VinP/N1           | VRP/N1 5-0 = 100000    | $((430R - 66R) / 450R) * (VREG1 - VGS) + VGS$  |
|                   | VRP/N1 5-0 = 100001    | $((430R - 70R) / 450R) * (VREG1 - VGS) + VGS$  |
|                   | VRP/N1 5-0 = 100010    | $((430R - 74R) / 450R) * (VREG1 - VGS) + VGS$  |
|                   | VRP/N1 5-0 = 100011    | $((430R - 78R) / 450R) * (VREG1 - VGS) + VGS$  |
|                   | VRP/N1 5-0 = 100100    | $((430R - 82R) / 450R) * (VREG1 - VGS) + VGS$  |
|                   | VRP/N1 5-0 = 100101    | $((430R - 86R) / 450R) * (VREG1 - VGS) + VGS$  |
|                   | VRP/N1 5-0 = 100110    | $((430R - 90R) / 450R) * (VREG1 - VGS) + VGS$  |
|                   | VRP/N1 5-0 = 100111    | $((430R - 94R) / 450R) * (VREG1 - VGS) + VGS$  |
|                   | VRP/N1 5-0 = 101000    | $((430R - 98R) / 450R) * (VREG1 - VGS) + VGS$  |
|                   | VRP/N1 5-0 = 101001    | $((430R - 102R) / 450R) * (VREG1 - VGS) + VGS$ |
|                   | VRP/N1 5-0 = 101010    | $((430R - 106R) / 450R) * (VREG1 - VGS) + VGS$ |
|                   | VRP/N1 5-0 = 101011    | $((430R - 110R) / 450R) * (VREG1 - VGS) + VGS$ |
|                   | VRP/N1 5-0 = 101100    | $((430R - 114R) / 450R) * (VREG1 - VGS) + VGS$ |
|                   | VRP/N1 5-0 = 101101    | $((430R - 118R) / 450R) * (VREG1 - VGS) + VGS$ |
|                   | VRP/N1 5-0 = 101110    | $((430R - 122R) / 450R) * (VREG1 - VGS) + VGS$ |
|                   | VRP/N1 5-0 = 101111    | $((430R - 126R) / 450R) * (VREG1 - VGS) + VGS$ |
|                   | VRP/N1 5-0 = 110000    | $((430R - 130R) / 450R) * (VREG1 - VGS) + VGS$ |
|                   | VRP/N1 5-0 = 110001    | $((430R - 134R) / 450R) * (VREG1 - VGS) + VGS$ |
|                   | VRP/N1 5-0 = 110010    | $((430R - 138R) / 450R) * (VREG1 - VGS) + VGS$ |
|                   | VRP/N1 5-0 = 110011    | $((430R - 142R) / 450R) * (VREG1 - VGS) + VGS$ |
|                   | VRP/N1 5-0 = 110100    | $((430R - 146R) / 450R) * (VREG1 - VGS) + VGS$ |
|                   | VRP/N1 5-0 = 110101    | $((430R - 150R) / 450R) * (VREG1 - VGS) + VGS$ |
|                   | VRP/N1 5-0 = 110110    | $((430R - 154R) / 450R) * (VREG1 - VGS) + VGS$ |
|                   | VRP/N1 5-0 = 110111    | $((430R - 158R) / 450R) * (VREG1 - VGS) + VGS$ |
|                   | VRP/N1 5-0 = 111000    | $((430R - 162R) / 450R) * (VREG1 - VGS) + VGS$ |
|                   | VRP/N1 5-0 = 111001    | $((430R - 166R) / 450R) * (VREG1 - VGS) + VGS$ |
|                   | VRP/N1 5-0 = 111010    | $((430R - 170R) / 450R) * (VREG1 - VGS) + VGS$ |
|                   | VRP/N1 5-0 = 111011    | $((430R - 174R) / 450R) * (VREG1 - VGS) + VGS$ |
|                   | VRP/N1 5-0 = 111100    | $((430R - 178R) / 450R) * (VREG1 - VGS) + VGS$ |
|                   | VRP/N1 5-0 = 111101    | $((430R - 182R) / 450R) * (VREG1 - VGS) + VGS$ |
|                   | VRP/N1 5-0 = 111110    | $((430R - 186R) / 450R) * (VREG1 - VGS) + VGS$ |
|                   | VRP/N1 5-0 = 111111    | $((430R - 190R) / 450R) * (VREG1 - VGS) + VGS$ |

Table 5.16: VinP/N 1

| Reference Voltage | Macro Adjustment Value | VinP/N2 Formula                                |
|-------------------|------------------------|--|
|                   | VRP/N2 5-0 = 000000    | $(410R / 450R) * (VREG1 - VGS) + VGS$          |
|                   | VRP/N2 5-0 = 000001    | $((410R - 2R) / 450R) * (VREG1 - VGS) + VGS$   |
|                   | VRP/N2 5-0 = 000010    | $((410R - 4R) / 450R) * (VREG1 - VGS) + VGS$   |
|                   | VRP/N2 5-0 = 000011    | $((410R - 6R) / 450R) * (VREG1 - VGS) + VGS$   |
|                   | VRP/N2 5-0 = 000100    | $((410R - 8R) / 450R) * (VREG1 - VGS) + VGS$   |
|                   | VRP/N2 5-0 = 000101    | $((410R - 10R) / 450R) * (VREG1 - VGS) + VGS$  |
|                   | VRP/N2 5-0 = 000110    | $((410R - 12R) / 450R) * (VREG1 - VGS) + VGS$  |
|                   | VRP/N2 5-0 = 000111    | $((410R - 14R) / 450R) * (VREG1 - VGS) + VGS$  |
|                   | VRP/N2 5-0 = 001000    | $((410R - 16R) / 450R) * (VREG1 - VGS) + VGS$  |
|                   | VRP/N2 5-0 = 001001    | $((410R - 18R) / 450R) * (VREG1 - VGS) + VGS$  |
|                   | VRP/N2 5-0 = 001010    | $((410R - 20R) / 450R) * (VREG1 - VGS) + VGS$  |
|                   | VRP/N2 5-0 = 001011    | $((410R - 22R) / 450R) * (VREG1 - VGS) + VGS$  |
|                   | VRP/N2 5-0 = 001100    | $((410R - 24R) / 450R) * (VREG1 - VGS) + VGS$  |
|                   | VRP/N2 5-0 = 001101    | $((410R - 26R) / 450R) * (VREG1 - VGS) + VGS$  |
|                   | VRP/N2 5-0 = 001110    | $((410R - 28R) / 450R) * (VREG1 - VGS) + VGS$  |
|                   | VRP/N2 5-0 = 001111    | $((410R - 30R) / 450R) * (VREG1 - VGS) + VGS$  |
|                   | VRP/N2 5-0 = 010000    | $((410R - 32R) / 450R) * (VREG1 - VGS) + VGS$  |
|                   | VRP/N2 5-0 = 010001    | $((410R - 34R) / 450R) * (VREG1 - VGS) + VGS$  |
|                   | VRP/N2 5-0 = 010010    | $((410R - 36R) / 450R) * (VREG1 - VGS) + VGS$  |
|                   | VRP/N2 5-0 = 010011    | $((410R - 38R) / 450R) * (VREG1 - VGS) + VGS$  |
|                   | VRP/N2 5-0 = 010100    | $((410R - 40R) / 450R) * (VREG1 - VGS) + VGS$  |
|                   | VRP/N2 5-0 = 010101    | $((410R - 42R) / 450R) * (VREG1 - VGS) + VGS$  |
|                   | VRP/N2 5-0 = 010110    | $((410R - 44R) / 450R) * (VREG1 - VGS) + VGS$  |
|                   | VRP/N2 5-0 = 010111    | $((410R - 46R) / 450R) * (VREG1 - VGS) + VGS$  |
|                   | VRP/N2 5-0 = 011000    | $((410R - 48R) / 450R) * (VREG1 - VGS) + VGS$  |
|                   | VRP/N2 5-0 = 011001    | $((410R - 50R) / 450R) * (VREG1 - VGS) + VGS$  |
|                   | VRP/N2 5-0 = 011010    | $((410R - 52R) / 450R) * (VREG1 - VGS) + VGS$  |
|                   | VRP/N2 5-0 = 011011    | $((410R - 54R) / 450R) * (VREG1 - VGS) + VGS$  |
|                   | VRP/N2 5-0 = 011100    | $((410R - 56R) / 450R) * (VREG1 - VGS) + VGS$  |
|                   | VRP/N2 5-0 = 011101    | $((410R - 58R) / 450R) * (VREG1 - VGS) + VGS$  |
|                   | VRP/N2 5-0 = 011110    | $((410R - 60R) / 450R) * (VREG1 - VGS) + VGS$  |
|                   | VRP/N2 5-0 = 011111    | $((410R - 62R) / 450R) * (VREG1 - VGS) + VGS$  |
| VinP/N2           | VRP/N2 5-0 = 100000    | $((410R - 66R) / 450R) * (VREG1 - VGS) + VGS$  |
|                   | VRP/N2 5-0 = 100001    | $((410R - 70R) / 450R) * (VREG1 - VGS) + VGS$  |
|                   | VRP/N2 5-0 = 100010    | $((410R - 74R) / 450R) * (VREG1 - VGS) + VGS$  |
|                   | VRP/N2 5-0 = 100011    | $((410R - 78R) / 450R) * (VREG1 - VGS) + VGS$  |
|                   | VRP/N2 5-0 = 100100    | $((410R - 82R) / 450R) * (VREG1 - VGS) + VGS$  |
|                   | VRP/N2 5-0 = 100101    | $((410R - 86R) / 450R) * (VREG1 - VGS) + VGS$  |
|                   | VRP/N2 5-0 = 100110    | $((410R - 90R) / 450R) * (VREG1 - VGS) + VGS$  |
|                   | VRP/N2 5-0 = 100111    | $((410R - 94R) / 450R) * (VREG1 - VGS) + VGS$  |
|                   | VRP/N2 5-0 = 101000    | $((410R - 98R) / 450R) * (VREG1 - VGS) + VGS$  |
|                   | VRP/N2 5-0 = 101001    | $((410R - 102R) / 450R) * (VREG1 - VGS) + VGS$ |
|                   | VRP/N2 5-0 = 101010    | $((410R - 106R) / 450R) * (VREG1 - VGS) + VGS$ |
|                   | VRP/N2 5-0 = 101011    | $((410R - 110R) / 450R) * (VREG1 - VGS) + VGS$ |
|                   | VRP/N2 5-0 = 101100    | $((410R - 114R) / 450R) * (VREG1 - VGS) + VGS$ |
|                   | VRP/N2 5-0 = 101101    | $((410R - 118R) / 450R) * (VREG1 - VGS) + VGS$ |
|                   | VRP/N2 5-0 = 101110    | $((410R - 122R) / 450R) * (VREG1 - VGS) + VGS$ |
|                   | VRP/N2 5-0 = 101111    | $((410R - 126R) / 450R) * (VREG1 - VGS) + VGS$ |
|                   | VRP/N2 5-0 = 110000    | $((410R - 130R) / 450R) * (VREG1 - VGS) + VGS$ |
|                   | VRP/N2 5-0 = 110001    | $((410R - 134R) / 450R) * (VREG1 - VGS) + VGS$ |
|                   | VRP/N2 5-0 = 110010    | $((410R - 138R) / 450R) * (VREG1 - VGS) + VGS$ |
|                   | VRP/N2 5-0 = 110011    | $((410R - 142R) / 450R) * (VREG1 - VGS) + VGS$ |
|                   | VRP/N2 5-0 = 110100    | $((410R - 146R) / 450R) * (VREG1 - VGS) + VGS$ |
|                   | VRP/N2 5-0 = 110101    | $((410R - 150R) / 450R) * (VREG1 - VGS) + VGS$ |
|                   | VRP/N2 5-0 = 110110    | $((410R - 154R) / 450R) * (VREG1 - VGS) + VGS$ |
|                   | VRP/N2 5-0 = 110111    | $((410R - 158R) / 450R) * (VREG1 - VGS) + VGS$ |
|                   | VRP/N2 5-0 = 111000    | $((410R - 162R) / 450R) * (VREG1 - VGS) + VGS$ |
|                   | VRP/N2 5-0 = 111001    | $((410R - 166R) / 450R) * (VREG1 - VGS) + VGS$ |
|                   | VRP/N2 5-0 = 111010    | $((410R - 170R) / 450R) * (VREG1 - VGS) + VGS$ |
|                   | VRP/N2 5-0 = 111011    | $((410R - 174R) / 450R) * (VREG1 - VGS) + VGS$ |
|                   | VRP/N2 5-0 = 111100    | $((410R - 178R) / 450R) * (VREG1 - VGS) + VGS$ |
|                   | VRP/N2 5-0 = 111101    | $((410R - 182R) / 450R) * (VREG1 - VGS) + VGS$ |
|                   | VRP/N2 5-0 = 111110    | $((410R - 186R) / 450R) * (VREG1 - VGS) + VGS$ |
|                   | VRP/N2 5-0 = 111111    | $((410R - 190R) / 450R) * (VREG1 - VGS) + VGS$ |

Table 5.17: VinP/N 2



| Reference Voltage | Macro Adjustment Value | VinP/N10 Formula                               |
|-------------------|------------------------|--|
|                   | VRP/N3 5-0 = 000000    | $(230R / 450R) * (VREG1 - VGS) + VGS$          |
|                   | VRP/N3 5-0 = 000001    | $((230R - 4R) / 450R) * (VREG1 - VGS) + VGS$   |
|                   | VRP/N3 5-0 = 000010    | $((230R - 8R) / 450R) * (VREG1 - VGS) + VGS$   |
|                   | VRP/N3 5-0 = 000011    | $((230R - 12R) / 450R) * (VREG1 - VGS) + VGS$  |
|                   | VRP/N3 5-0 = 000100    | $((230R - 16R) / 450R) * (VREG1 - VGS) + VGS$  |
|                   | VRP/N3 5-0 = 000101    | $((230R - 20R) / 450R) * (VREG1 - VGS) + VGS$  |
|                   | VRP/N3 5-0 = 000110    | $((230R - 24R) / 450R) * (VREG1 - VGS) + VGS$  |
|                   | VRP/N3 5-0 = 000111    | $((230R - 28R) / 450R) * (VREG1 - VGS) + VGS$  |
|                   | VRP/N3 5-0 = 001000    | $((230R - 32R) / 450R) * (VREG1 - VGS) + VGS$  |
|                   | VRP/N3 5-0 = 001001    | $((230R - 36R) / 450R) * (VREG1 - VGS) + VGS$  |
|                   | VRP/N3 5-0 = 001010    | $((230R - 40R) / 450R) * (VREG1 - VGS) + VGS$  |
|                   | VRP/N3 5-0 = 001011    | $((230R - 44R) / 450R) * (VREG1 - VGS) + VGS$  |
|                   | VRP/N3 5-0 = 001100    | $((230R - 48R) / 450R) * (VREG1 - VGS) + VGS$  |
|                   | VRP/N3 5-0 = 001101    | $((230R - 52R) / 450R) * (VREG1 - VGS) + VGS$  |
|                   | VRP/N3 5-0 = 001110    | $((230R - 56R) / 450R) * (VREG1 - VGS) + VGS$  |
|                   | VRP/N3 5-0 = 001111    | $((230R - 60R) / 450R) * (VREG1 - VGS) + VGS$  |
|                   | VRP/N3 5-0 = 010000    | $((230R - 64R) / 450R) * (VREG1 - VGS) + VGS$  |
|                   | VRP/N3 5-0 = 010001    | $((230R - 68R) / 450R) * (VREG1 - VGS) + VGS$  |
|                   | VRP/N3 5-0 = 010010    | $((230R - 72R) / 450R) * (VREG1 - VGS) + VGS$  |
|                   | VRP/N3 5-0 = 010011    | $((230R - 76R) / 450R) * (VREG1 - VGS) + VGS$  |
|                   | VRP/N3 5-0 = 010100    | $((230R - 80R) / 450R) * (VREG1 - VGS) + VGS$  |
|                   | VRP/N3 5-0 = 010101    | $((230R - 84R) / 450R) * (VREG1 - VGS) + VGS$  |
|                   | VRP/N3 5-0 = 010110    | $((230R - 88R) / 450R) * (VREG1 - VGS) + VGS$  |
|                   | VRP/N3 5-0 = 010111    | $((230R - 92R) / 450R) * (VREG1 - VGS) + VGS$  |
|                   | VRP/N3 5-0 = 011000    | $((230R - 96R) / 450R) * (VREG1 - VGS) + VGS$  |
|                   | VRP/N3 5-0 = 011001    | $((230R - 100R) / 450R) * (VREG1 - VGS) + VGS$ |
|                   | VRP/N3 5-0 = 011010    | $((230R - 104R) / 450R) * (VREG1 - VGS) + VGS$ |
|                   | VRP/N3 5-0 = 011011    | $((230R - 108R) / 450R) * (VREG1 - VGS) + VGS$ |
|                   | VRP/N3 5-0 = 011100    | $((230R - 112R) / 450R) * (VREG1 - VGS) + VGS$ |
|                   | VRP/N3 5-0 = 011101    | $((230R - 116R) / 450R) * (VREG1 - VGS) + VGS$ |
|                   | VRP/N3 5-0 = 011110    | $((230R - 120R) / 450R) * (VREG1 - VGS) + VGS$ |
|                   | VRP/N3 5-0 = 011111    | $((230R - 124R) / 450R) * (VREG1 - VGS) + VGS$ |
| VinP/N10          | VRP/N3 5-0 = 100000    | $((230R - 128R) / 450R) * (VREG1 - VGS) + VGS$ |
|                   | VRP/N3 5-0 = 100001    | $((230R - 130R) / 450R) * (VREG1 - VGS) + VGS$ |
|                   | VRP/N3 5-0 = 100010    | $((230R - 132R) / 450R) * (VREG1 - VGS) + VGS$ |
|                   | VRP/N3 5-0 = 100011    | $((230R - 134R) / 450R) * (VREG1 - VGS) + VGS$ |
|                   | VRP/N3 5-0 = 100100    | $((230R - 136R) / 450R) * (VREG1 - VGS) + VGS$ |
|                   | VRP/N3 5-0 = 100101    | $((230R - 138R) / 450R) * (VREG1 - VGS) + VGS$ |
|                   | VRP/N3 5-0 = 100110    | $((230R - 140R) / 450R) * (VREG1 - VGS) + VGS$ |
|                   | VRP/N3 5-0 = 100111    | $((230R - 142R) / 450R) * (VREG1 - VGS) + VGS$ |
|                   | VRP/N3 5-0 = 101000    | $((230R - 144R) / 450R) * (VREG1 - VGS) + VGS$ |
|                   | VRP/N3 5-0 = 101001    | $((230R - 146R) / 450R) * (VREG1 - VGS) + VGS$ |
|                   | VRP/N3 5-0 = 101010    | $((230R - 148R) / 450R) * (VREG1 - VGS) + VGS$ |
|                   | VRP/N3 5-0 = 101011    | $((230R - 150R) / 450R) * (VREG1 - VGS) + VGS$ |
|                   | VRP/N3 5-0 = 101100    | $((230R - 152R) / 450R) * (VREG1 - VGS) + VGS$ |
|                   | VRP/N3 5-0 = 101101    | $((230R - 154R) / 450R) * (VREG1 - VGS) + VGS$ |
|                   | VRP/N3 5-0 = 101110    | $((230R - 156R) / 450R) * (VREG1 - VGS) + VGS$ |
|                   | VRP/N3 5-0 = 101111    | $((230R - 158R) / 450R) * (VREG1 - VGS) + VGS$ |
|                   | VRP/N3 5-0 = 110000    | $((230R - 160R) / 450R) * (VREG1 - VGS) + VGS$ |
|                   | VRP/N3 5-0 = 110001    | $((230R - 162R) / 450R) * (VREG1 - VGS) + VGS$ |
|                   | VRP/N3 5-0 = 110010    | $((230R - 164R) / 450R) * (VREG1 - VGS) + VGS$ |
|                   | VRP/N3 5-0 = 110011    | $((230R - 166R) / 450R) * (VREG1 - VGS) + VGS$ |
|                   | VRP/N3 5-0 = 110100    | $((230R - 168R) / 450R) * (VREG1 - VGS) + VGS$ |
|                   | VRP/N3 5-0 = 110101    | $((230R - 170R) / 450R) * (VREG1 - VGS) + VGS$ |
|                   | VRP/N3 5-0 = 110110    | $((230R - 172R) / 450R) * (VREG1 - VGS) + VGS$ |
|                   | VRP/N3 5-0 = 110111    | $((230R - 174R) / 450R) * (VREG1 - VGS) + VGS$ |
|                   | VRP/N3 5-0 = 111000    | $((230R - 176R) / 450R) * (VREG1 - VGS) + VGS$ |
|                   | VRP/N3 5-0 = 111001    | $((230R - 178R) / 450R) * (VREG1 - VGS) + VGS$ |
|                   | VRP/N3 5-0 = 111010    | $((230R - 180R) / 450R) * (VREG1 - VGS) + VGS$ |
|                   | VRP/N3 5-0 = 111011    | $((230R - 182R) / 450R) * (VREG1 - VGS) + VGS$ |
|                   | VRP/N3 5-0 = 111100    | $((230R - 184R) / 450R) * (VREG1 - VGS) + VGS$ |
|                   | VRP/N3 5-0 = 111101    | $((230R - 186R) / 450R) * (VREG1 - VGS) + VGS$ |
|                   | VRP/N3 5-0 = 111110    | $((230R - 188R) / 450R) * (VREG1 - VGS) + VGS$ |
|                   | VRP/N3 5-0 = 111111    | $((230R - 190R) / 450R) * (VREG1 - VGS) + VGS$ |

Table 5.18: VinP/N 10

| Reference Voltage   | Macro Adjustment Value                         | VinP/N11 Formula                               |
|---------------------|--|--|
| VinP/N11            | VRP/N4 5-0 = 000000                            | $(210R / 450R) * (VREG1 - VGS) + VGS$          |
|                     | VRP/N4 5-0 = 000001                            | $((210R - 4R) / 450R) * (VREG1 - VGS) + VGS$   |
|                     | VRP/N4 5-0 = 000010                            | $((210R - 8R) / 450R) * (VREG1 - VGS) + VGS$   |
|                     | VRP/N4 5-0 = 000011                            | $((210R - 12R) / 450R) * (VREG1 - VGS) + VGS$  |
|                     | VRP/N4 5-0 = 000100                            | $((210R - 16R) / 450R) * (VREG1 - VGS) + VGS$  |
|                     | VRP/N4 5-0 = 000101                            | $((210R - 20R) / 450R) * (VREG1 - VGS) + VGS$  |
|                     | VRP/N4 5-0 = 000110                            | $((210R - 24R) / 450R) * (VREG1 - VGS) + VGS$  |
|                     | VRP/N4 5-0 = 000111                            | $((210R - 28R) / 450R) * (VREG1 - VGS) + VGS$  |
|                     | VRP/N4 5-0 = 001000                            | $((210R - 32R) / 450R) * (VREG1 - VGS) + VGS$  |
|                     | VRP/N4 5-0 = 001001                            | $((210R - 36R) / 450R) * (VREG1 - VGS) + VGS$  |
|                     | VRP/N4 5-0 = 001010                            | $((210R - 40R) / 450R) * (VREG1 - VGS) + VGS$  |
|                     | VRP/N4 5-0 = 001011                            | $((210R - 44R) / 450R) * (VREG1 - VGS) + VGS$  |
|                     | VRP/N4 5-0 = 001100                            | $((210R - 48R) / 450R) * (VREG1 - VGS) + VGS$  |
|                     | VRP/N4 5-0 = 001101                            | $((210R - 52R) / 450R) * (VREG1 - VGS) + VGS$  |
|                     | VRP/N4 5-0 = 001110                            | $((210R - 56R) / 450R) * (VREG1 - VGS) + VGS$  |
|                     | VRP/N4 5-0 = 001111                            | $((210R - 60R) / 450R) * (VREG1 - VGS) + VGS$  |
|                     | VRP/N4 5-0 = 010000                            | $((210R - 64R) / 450R) * (VREG1 - VGS) + VGS$  |
|                     | VRP/N4 5-0 = 010001                            | $((210R - 68R) / 450R) * (VREG1 - VGS) + VGS$  |
|                     | VRP/N4 5-0 = 010010                            | $((210R - 72R) / 450R) * (VREG1 - VGS) + VGS$  |
|                     | VRP/N4 5-0 = 010011                            | $((210R - 76R) / 450R) * (VREG1 - VGS) + VGS$  |
|                     | VRP/N4 5-0 = 010100                            | $((210R - 80R) / 450R) * (VREG1 - VGS) + VGS$  |
|                     | VRP/N4 5-0 = 010101                            | $((210R - 84R) / 450R) * (VREG1 - VGS) + VGS$  |
|                     | VRP/N4 5-0 = 010110                            | $((210R - 88R) / 450R) * (VREG1 - VGS) + VGS$  |
|                     | VRP/N4 5-0 = 010111                            | $((210R - 92R) / 450R) * (VREG1 - VGS) + VGS$  |
|                     | VRP/N4 5-0 = 011000                            | $((210R - 96R) / 450R) * (VREG1 - VGS) + VGS$  |
|                     | VRP/N4 5-0 = 011001                            | $((210R - 100R) / 450R) * (VREG1 - VGS) + VGS$ |
|                     | VRP/N4 5-0 = 011010                            | $((210R - 104R) / 450R) * (VREG1 - VGS) + VGS$ |
|                     | VRP/N4 5-0 = 011011                            | $((210R - 108R) / 450R) * (VREG1 - VGS) + VGS$ |
|                     | VRP/N4 5-0 = 011100                            | $((210R - 112R) / 450R) * (VREG1 - VGS) + VGS$ |
|                     | VRP/N4 5-0 = 011101                            | $((210R - 116R) / 450R) * (VREG1 - VGS) + VGS$ |
|                     | VRP/N4 5-0 = 011110                            | $((210R - 120R) / 450R) * (VREG1 - VGS) + VGS$ |
|                     | VRP/N4 5-0 = 011111                            | $((210R - 124R) / 450R) * (VREG1 - VGS) + VGS$ |
|                     | VRP/N4 5-0 = 100000                            | $((210R - 128R) / 450R) * (VREG1 - VGS) + VGS$ |
|                     | VRP/N4 5-0 = 100001                            | $((210R - 130R) / 450R) * (VREG1 - VGS) + VGS$ |
|                     | VRP/N4 5-0 = 100010                            | $((210R - 132R) / 450R) * (VREG1 - VGS) + VGS$ |
|                     | VRP/N4 5-0 = 100011                            | $((210R - 134R) / 450R) * (VREG1 - VGS) + VGS$ |
|                     | VRP/N4 5-0 = 100100                            | $((210R - 136R) / 450R) * (VREG1 - VGS) + VGS$ |
|                     | VRP/N4 5-0 = 100101                            | $((210R - 138R) / 450R) * (VREG1 - VGS) + VGS$ |
|                     | VRP/N4 5-0 = 100110                            | $((210R - 140R) / 450R) * (VREG1 - VGS) + VGS$ |
|                     | VRP/N4 5-0 = 100111                            | $((210R - 142R) / 450R) * (VREG1 - VGS) + VGS$ |
| VRP/N4 5-0 = 101000 | $((210R - 144R) / 450R) * (VREG1 - VGS) + VGS$ |  |
| VRP/N4 5-0 = 101001 | $((210R - 146R) / 450R) * (VREG1 - VGS) + VGS$ |  |
| VRP/N4 5-0 = 101010 | $((210R - 148R) / 450R) * (VREG1 - VGS) + VGS$ |  |
| VRP/N4 5-0 = 101011 | $((210R - 150R) / 450R) * (VREG1 - VGS) + VGS$ |  |
| VRP/N4 5-0 = 101100 | $((210R - 152R) / 450R) * (VREG1 - VGS) + VGS$ |  |
| VRP/N4 5-0 = 101101 | $((210R - 154R) / 450R) * (VREG1 - VGS) + VGS$ |  |
| VRP/N4 5-0 = 101110 | $((210R - 156R) / 450R) * (VREG1 - VGS) + VGS$ |  |
| VRP/N4 5-0 = 101111 | $((210R - 158R) / 450R) * (VREG1 - VGS) + VGS$ |  |
| VRP/N4 5-0 = 110000 | $((210R - 160R) / 450R) * (VREG1 - VGS) + VGS$ |  |
| VRP/N4 5-0 = 110001 | $((210R - 162R) / 450R) * (VREG1 - VGS) + VGS$ |  |
| VRP/N4 5-0 = 110010 | $((210R - 164R) / 450R) * (VREG1 - VGS) + VGS$ |  |
| VRP/N4 5-0 = 110011 | $((210R - 166R) / 450R) * (VREG1 - VGS) + VGS$ |  |
| VRP/N4 5-0 = 110100 | $((210R - 168R) / 450R) * (VREG1 - VGS) + VGS$ |  |
| VRP/N4 5-0 = 110101 | $((210R - 170R) / 450R) * (VREG1 - VGS) + VGS$ |  |
| VRP/N4 5-0 = 110110 | $((210R - 172R) / 450R) * (VREG1 - VGS) + VGS$ |  |
| VRP/N4 5-0 = 110111 | $((210R - 174R) / 450R) * (VREG1 - VGS) + VGS$ |  |
| VRP/N4 5-0 = 111000 | $((210R - 176R) / 450R) * (VREG1 - VGS) + VGS$ |  |
| VRP/N4 5-0 = 111001 | $((210R - 178R) / 450R) * (VREG1 - VGS) + VGS$ |  |
| VRP/N4 5-0 = 111010 | $((210R - 180R) / 450R) * (VREG1 - VGS) + VGS$ |  |
| VRP/N4 5-0 = 111011 | $((210R - 182R) / 450R) * (VREG1 - VGS) + VGS$ |  |
| VRP/N4 5-0 = 111100 | $((210R - 184R) / 450R) * (VREG1 - VGS) + VGS$ |  |
| VRP/N4 5-0 = 111101 | $((210R - 186R) / 450R) * (VREG1 - VGS) + VGS$ |  |
| VRP/N4 5-0 = 111110 | $((210R - 188R) / 450R) * (VREG1 - VGS) + VGS$ |  |
| VRP/N4 5-0 = 111111 | $((210R - 190R) / 450R) * (VREG1 - VGS) + VGS$ |  |

Table 5.19: VinP/N 11

| Reference Voltage | Macro Adjustment Value | VinP/N12 Formula                               |
|-------------------|------------------------|--|
|                   | VRP/N5 5-0 = 000000    | $(210R / 450R) * (VREG1 - VGS) + VGS$          |
|                   | VRP/N5 5-0 = 000001    | $((208R - 4R) / 450R) * (VREG1 - VGS) + VGS$   |
|                   | VRP/N5 5-0 = 000010    | $((208R - 8R) / 450R) * (VREG1 - VGS) + VGS$   |
|                   | VRP/N5 5-0 = 000011    | $((208R - 12R) / 450R) * (VREG1 - VGS) + VGS$  |
|                   | VRP/N5 5-0 = 000100    | $((208R - 16R) / 450R) * (VREG1 - VGS) + VGS$  |
|                   | VRP/N5 5-0 = 000101    | $((208R - 20R) / 450R) * (VREG1 - VGS) + VGS$  |
|                   | VRP/N5 5-0 = 000110    | $((208R - 24R) / 450R) * (VREG1 - VGS) + VGS$  |
|                   | VRP/N5 5-0 = 000111    | $((208R - 28R) / 450R) * (VREG1 - VGS) + VGS$  |
|                   | VRP/N5 5-0 = 001000    | $((208R - 32R) / 450R) * (VREG1 - VGS) + VGS$  |
|                   | VRP/N5 5-0 = 001001    | $((208R - 36R) / 450R) * (VREG1 - VGS) + VGS$  |
|                   | VRP/N5 5-0 = 001010    | $((208R - 40R) / 450R) * (VREG1 - VGS) + VGS$  |
|                   | VRP/N5 5-0 = 001011    | $((208R - 44R) / 450R) * (VREG1 - VGS) + VGS$  |
|                   | VRP/N5 5-0 = 001100    | $((208R - 48R) / 450R) * (VREG1 - VGS) + VGS$  |
|                   | VRP/N5 5-0 = 001101    | $((208R - 52R) / 450R) * (VREG1 - VGS) + VGS$  |
|                   | VRP/N5 5-0 = 001110    | $((208R - 56R) / 450R) * (VREG1 - VGS) + VGS$  |
|                   | VRP/N5 5-0 = 001111    | $((208R - 60R) / 450R) * (VREG1 - VGS) + VGS$  |
|                   | VRP/N5 5-0 = 010000    | $((208R - 64R) / 450R) * (VREG1 - VGS) + VGS$  |
|                   | VRP/N5 5-0 = 010001    | $((208R - 68R) / 450R) * (VREG1 - VGS) + VGS$  |
|                   | VRP/N5 5-0 = 010010    | $((208R - 72R) / 450R) * (VREG1 - VGS) + VGS$  |
|                   | VRP/N5 5-0 = 010011    | $((208R - 76R) / 450R) * (VREG1 - VGS) + VGS$  |
|                   | VRP/N5 5-0 = 010100    | $((208R - 80R) / 450R) * (VREG1 - VGS) + VGS$  |
|                   | VRP/N5 5-0 = 010101    | $((208R - 84R) / 450R) * (VREG1 - VGS) + VGS$  |
|                   | VRP/N5 5-0 = 010110    | $((208R - 88R) / 450R) * (VREG1 - VGS) + VGS$  |
|                   | VRP/N5 5-0 = 010111    | $((208R - 92R) / 450R) * (VREG1 - VGS) + VGS$  |
|                   | VRP/N5 5-0 = 011000    | $((208R - 96R) / 450R) * (VREG1 - VGS) + VGS$  |
|                   | VRP/N5 5-0 = 011001    | $((208R - 100R) / 450R) * (VREG1 - VGS) + VGS$ |
|                   | VRP/N5 5-0 = 011010    | $((208R - 104R) / 450R) * (VREG1 - VGS) + VGS$ |
|                   | VRP/N5 5-0 = 011011    | $((208R - 108R) / 450R) * (VREG1 - VGS) + VGS$ |
|                   | VRP/N5 5-0 = 011100    | $((208R - 112R) / 450R) * (VREG1 - VGS) + VGS$ |
|                   | VRP/N5 5-0 = 011101    | $((208R - 116R) / 450R) * (VREG1 - VGS) + VGS$ |
|                   | VRP/N5 5-0 = 011110    | $((208R - 120R) / 450R) * (VREG1 - VGS) + VGS$ |
|                   | VRP/N5 5-0 = 011111    | $((208R - 124R) / 450R) * (VREG1 - VGS) + VGS$ |
| VinP/N12          | VRP/N5 5-0 = 100000    | $((208R - 128R) / 450R) * (VREG1 - VGS) + VGS$ |
|                   | VRP/N5 5-0 = 100001    | $((208R - 130R) / 450R) * (VREG1 - VGS) + VGS$ |
|                   | VRP/N5 5-0 = 100010    | $((208R - 132R) / 450R) * (VREG1 - VGS) + VGS$ |
|                   | VRP/N5 5-0 = 100011    | $((208R - 134R) / 450R) * (VREG1 - VGS) + VGS$ |
|                   | VRP/N5 5-0 = 100100    | $((208R - 136R) / 450R) * (VREG1 - VGS) + VGS$ |
|                   | VRP/N5 5-0 = 100101    | $((208R - 138R) / 450R) * (VREG1 - VGS) + VGS$ |
|                   | VRP/N5 5-0 = 100110    | $((208R - 140R) / 450R) * (VREG1 - VGS) + VGS$ |
|                   | VRP/N5 5-0 = 100111    | $((208R - 142R) / 450R) * (VREG1 - VGS) + VGS$ |
|                   | VRP/N5 5-0 = 101000    | $((208R - 144R) / 450R) * (VREG1 - VGS) + VGS$ |
|                   | VRP/N5 5-0 = 101001    | $((208R - 146R) / 450R) * (VREG1 - VGS) + VGS$ |
|                   | VRP/N5 5-0 = 101010    | $((208R - 148R) / 450R) * (VREG1 - VGS) + VGS$ |
|                   | VRP/N5 5-0 = 101011    | $((208R - 150R) / 450R) * (VREG1 - VGS) + VGS$ |
|                   | VRP/N5 5-0 = 101100    | $((208R - 152R) / 450R) * (VREG1 - VGS) + VGS$ |
|                   | VRP/N5 5-0 = 101101    | $((208R - 154R) / 450R) * (VREG1 - VGS) + VGS$ |
|                   | VRP/N5 5-0 = 101110    | $((208R - 156R) / 450R) * (VREG1 - VGS) + VGS$ |
|                   | VRP/N5 5-0 = 101111    | $((208R - 158R) / 450R) * (VREG1 - VGS) + VGS$ |
|                   | VRP/N5 5-0 = 110000    | $((208R - 160R) / 450R) * (VREG1 - VGS) + VGS$ |
|                   | VRP/N5 5-0 = 110001    | $((208R - 162R) / 450R) * (VREG1 - VGS) + VGS$ |
|                   | VRP/N5 5-0 = 110010    | $((208R - 164R) / 450R) * (VREG1 - VGS) + VGS$ |
|                   | VRP/N5 5-0 = 110011    | $((208R - 166R) / 450R) * (VREG1 - VGS) + VGS$ |
|                   | VRP/N5 5-0 = 110100    | $((208R - 168R) / 450R) * (VREG1 - VGS) + VGS$ |
|                   | VRP/N5 5-0 = 110101    | $((208R - 170R) / 450R) * (VREG1 - VGS) + VGS$ |
|                   | VRP/N5 5-0 = 110110    | $((208R - 172R) / 450R) * (VREG1 - VGS) + VGS$ |
|                   | VRP/N5 5-0 = 110111    | $((208R - 174R) / 450R) * (VREG1 - VGS) + VGS$ |
|                   | VRP/N5 5-0 = 111000    | $((208R - 176R) / 450R) * (VREG1 - VGS) + VGS$ |
|                   | VRP/N5 5-0 = 111001    | $((208R - 178R) / 450R) * (VREG1 - VGS) + VGS$ |
|                   | VRP/N5 5-0 = 111010    | $((208R - 180R) / 450R) * (VREG1 - VGS) + VGS$ |
|                   | VRP/N5 5-0 = 111011    | $((208R - 182R) / 450R) * (VREG1 - VGS) + VGS$ |
|                   | VRP/N5 5-0 = 111100    | $((208R - 184R) / 450R) * (VREG1 - VGS) + VGS$ |
|                   | VRP/N5 5-0 = 111101    | $((208R - 186R) / 450R) * (VREG1 - VGS) + VGS$ |
|                   | VRP/N5 5-0 = 111110    | $((208R - 188R) / 450R) * (VREG1 - VGS) + VGS$ |
|                   | VRP/N5 5-0 = 111111    | VGS  |

Table 5.20: VinP/N 12

| Reference Voltage    | Macro Adjustment Value                         | VinP/N4 Formula                               |
|----------------------|--|---|
| VinP/N4              | PRP/N0 6-0 = 0000000                           | $(350R / 450R) (VREG1 - VGS) + VGS$           |
|                      | PRP/N0 6-0 = 0000001                           | $((350R - 2R) / 450R) * (VREG1 - VGS) + VGS$  |
|                      | PRP/N0 6-0 = 0000010                           | $((350R - 4R) / 450R) * (VREG1 - VGS) + VGS$  |
|                      | PRP/N0 6-0 = 0000011                           | $((350R - 6R) / 450R) * (VREG1 - VGS) + VGS$  |
|                      | PRP/N0 6-0 = 0000100                           | $((350R - 8R) / 450R) * (VREG1 - VGS) + VGS$  |
|                      | PRP/N0 6-0 = 0000101                           | $((350R - 10R) / 450R) * (VREG1 - VGS) + VGS$ |
|                      | PRP/N0 6-0 = 0000110                           | $((350R - 12R) / 450R) * (VREG1 - VGS) + VGS$ |
|                      | PRP/N0 6-0 = 0000111                           | $((350R - 14R) / 450R) * (VREG1 - VGS) + VGS$ |
|                      | PRP/N0 6-0 = 0001000                           | $((350R - 16R) / 450R) * (VREG1 - VGS) + VGS$ |
|                      | PRP/N0 6-0 = 0001001                           | $((350R - 18R) / 450R) * (VREG1 - VGS) + VGS$ |
|                      | PRP/N0 6-0 = 0001010                           | $((350R - 20R) / 450R) * (VREG1 - VGS) + VGS$ |
|                      | PRP/N0 6-0 = 0001011                           | $((350R - 22R) / 450R) * (VREG1 - VGS) + VGS$ |
|                      | PRP/N0 6-0 = 0001100                           | $((350R - 24R) / 450R) * (VREG1 - VGS) + VGS$ |
|                      | PRP/N0 6-0 = 0001101                           | $((350R - 26R) / 450R) * (VREG1 - VGS) + VGS$ |
|                      | PRP/N0 6-0 = 0001110                           | $((350R - 28R) / 450R) * (VREG1 - VGS) + VGS$ |
|                      | PRP/N0 6-0 = 0001111                           | $((350R - 30R) / 450R) * (VREG1 - VGS) + VGS$ |
|                      | PRP/N0 6-0 = 0010000                           | $((350R - 32R) / 450R) * (VREG1 - VGS) + VGS$ |
|                      | PRP/N0 6-0 = 0010001                           | $((350R - 34R) / 450R) * (VREG1 - VGS) + VGS$ |
|                      | PRP/N0 6-0 = 0010010                           | $((350R - 36R) / 450R) * (VREG1 - VGS) + VGS$ |
|                      | PRP/N0 6-0 = 0010011                           | $((350R - 38R) / 450R) * (VREG1 - VGS) + VGS$ |
|                      | PRP/N0 6-0 = 0010100                           | $((350R - 40R) / 450R) * (VREG1 - VGS) + VGS$ |
|                      | PRP/N0 6-0 = 0010101                           | $((350R - 42R) / 450R) * (VREG1 - VGS) + VGS$ |
|                      | PRP/N0 6-0 = 0010110                           | $((350R - 44R) / 450R) * (VREG1 - VGS) + VGS$ |
|                      | PRP/N0 6-0 = 0010111                           | $((350R - 46R) / 450R) * (VREG1 - VGS) + VGS$ |
|                      | PRP/N0 6-0 = 0011000                           | $((350R - 48R) / 450R) * (VREG1 - VGS) + VGS$ |
|                      | PRP/N0 6-0 = 0011001                           | $((350R - 50R) / 450R) * (VREG1 - VGS) + VGS$ |
|                      | PRP/N0 6-0 = 0011010                           | $((350R - 52R) / 450R) * (VREG1 - VGS) + VGS$ |
|                      | PRP/N0 6-0 = 0011011                           | $((350R - 54R) / 450R) * (VREG1 - VGS) + VGS$ |
|                      | PRP/N0 6-0 = 0011100                           | $((350R - 56R) / 450R) * (VREG1 - VGS) + VGS$ |
|                      | PRP/N0 6-0 = 0011101                           | $((350R - 58R) / 450R) * (VREG1 - VGS) + VGS$ |
|                      | PRP/N0 6-0 = 0011110                           | $((350R - 60R) / 450R) * (VREG1 - VGS) + VGS$ |
|                      | PRP/N0 6-0 = 0011111                           | $((350R - 62R) / 450R) * (VREG1 - VGS) + VGS$ |
|                      | PRP/N0 6-0 = 0100000                           | $((350R - 64R) / 450R) * (VREG1 - VGS) + VGS$ |
|                      | PRP/N0 6-0 = 0100001                           | $((350R - 66R) / 450R) * (VREG1 - VGS) + VGS$ |
|                      | PRP/N0 6-0 = 0100010                           | $((350R - 68R) / 450R) * (VREG1 - VGS) + VGS$ |
|                      | PRP/N0 6-0 = 0100011                           | $((350R - 70R) / 450R) * (VREG1 - VGS) + VGS$ |
|                      | PRP/N0 6-0 = 0100100                           | $((350R - 72R) / 450R) * (VREG1 - VGS) + VGS$ |
|                      | PRP/N0 6-0 = 0100101                           | $((350R - 74R) / 450R) * (VREG1 - VGS) + VGS$ |
|                      | PRP/N0 6-0 = 0100110                           | $((350R - 76R) / 450R) * (VREG1 - VGS) + VGS$ |
|                      | PRP/N0 6-0 = 0100111                           | $((350R - 78R) / 450R) * (VREG1 - VGS) + VGS$ |
|                      | PRP/N0 6-0 = 0101000                           | $((350R - 80R) / 450R) * (VREG1 - VGS) + VGS$ |
|                      | PRP/N0 6-0 = 0101001                           | $((350R - 82R) / 450R) * (VREG1 - VGS) + VGS$ |
|                      | PRP/N0 6-0 = 0101010                           | $((350R - 84R) / 450R) * (VREG1 - VGS) + VGS$ |
|                      | PRP/N0 6-0 = 0101011                           | $((350R - 86R) / 450R) * (VREG1 - VGS) + VGS$ |
|                      | PRP/N0 6-0 = 0101100                           | $((350R - 88R) / 450R) * (VREG1 - VGS) + VGS$ |
|                      | PRP/N0 6-0 = 0101101                           | $((350R - 90R) / 450R) * (VREG1 - VGS) + VGS$ |
|                      | PRP/N0 6-0 = 0101110                           | $((350R - 92R) / 450R) * (VREG1 - VGS) + VGS$ |
|                      | PRP/N0 6-0 = 0101111                           | $((350R - 94R) / 450R) * (VREG1 - VGS) + VGS$ |
| PRP/N0 6-0 = 0110000 | $((350R - 96R) / 450R) * (VREG1 - VGS) + VGS$  |   |
| PRP/N0 6-0 = 0110001 | $((350R - 98R) / 450R) * (VREG1 - VGS) + VGS$  |   |
| PRP/N0 6-0 = 0110010 | $((350R - 100R) / 450R) * (VREG1 - VGS) + VGS$ |   |
| PRP/N0 6-0 = 0110011 | $((350R - 102R) / 450R) * (VREG1 - VGS) + VGS$ |   |
| PRP/N0 6-0 = 0110100 | $((350R - 104R) / 450R) * (VREG1 - VGS) + VGS$ |   |
| PRP/N0 6-0 = 0110101 | $((350R - 106R) / 450R) * (VREG1 - VGS) + VGS$ |   |
| PRP/N0 6-0 = 0110110 | $((350R - 108R) / 450R) * (VREG1 - VGS) + VGS$ |   |
| PRP/N0 6-0 = 0110111 | $((350R - 110R) / 450R) * (VREG1 - VGS) + VGS$ |   |
| PRP/N0 6-0 = 0111000 | $((350R - 112R) / 450R) * (VREG1 - VGS) + VGS$ |   |
| PRP/N0 6-0 = 0111001 | $((350R - 114R) / 450R) * (VREG1 - VGS) + VGS$ |   |
| PRP/N0 6-0 = 0111010 | $((350R - 116R) / 450R) * (VREG1 - VGS) + VGS$ |   |
| PRP/N0 6-0 = 0111011 | $((350R - 118R) / 450R) * (VREG1 - VGS) + VGS$ |   |
| PRP/N0 6-0 = 0111100 | $((350R - 120R) / 450R) * (VREG1 - VGS) + VGS$ |   |
| PRP/N0 6-0 = 0111101 | $((350R - 122R) / 450R) * (VREG1 - VGS) + VGS$ |   |
| PRP/N0 6-0 = 0111110 | $((350R - 124R) / 450R) * (VREG1 - VGS) + VGS$ |   |
| PRP/N0 6-0 = 0111111 | $((350R - 126R) / 450R) * (VREG1 - VGS) + VGS$ |   |
| PRP/N0 6-0 = 1000000 | $((350R - 128R) / 450R) * (VREG1 - VGS) + VGS$ |   |
| PRP/N0 6-0 = 1000001 | $((350R - 130R) / 450R) * (VREG1 - VGS) + VGS$ |   |
| PRP/N0 6-0 = 1000010 | $((350R - 132R) / 450R) * (VREG1 - VGS) + VGS$ |   |
| PRP/N0 6-0 = 1000011 | $((350R - 134R) / 450R) * (VREG1 - VGS) + VGS$ |   |
| PRP/N0 6-0 = 1000100 | $((350R - 136R) / 450R) * (VREG1 - VGS) + VGS$ |   |



| Reference Voltage | Macro Adjustment Value | VinP/N4 Formula                                |
|-------------------|------------------------|--|
|                   | PRP/N0 6-0 = 1000101   | $((350R - 138R) / 450R) * (VREG1 - VGS) + VGS$ |
|                   | PRP/N0 6-0 = 1000110   | $((350R - 140R) / 450R) * (VREG1 - VGS) + VGS$ |
|                   | PRP/N0 6-0 = 1000111   | $((350R - 142R) / 450R) * (VREG1 - VGS) + VGS$ |
|                   | PRP/N0 6-0 = 1001000   | $((350R - 144R) / 450R) * (VREG1 - VGS) + VGS$ |
|                   | PRP/N0 6-0 = 1001001   | $((350R - 146R) / 450R) * (VREG1 - VGS) + VGS$ |
|                   | PRP/N0 6-0 = 1001010   | $((350R - 148R) / 450R) * (VREG1 - VGS) + VGS$ |
|                   | PRP/N0 6-0 = 1001011   | $((350R - 150R) / 450R) * (VREG1 - VGS) + VGS$ |
|                   | PRP/N0 6-0 = 1001100   | $((350R - 152R) / 450R) * (VREG1 - VGS) + VGS$ |
|                   | PRP/N0 6-0 = 1001101   | $((350R - 154R) / 450R) * (VREG1 - VGS) + VGS$ |
|                   | PRP/N0 6-0 = 1001110   | $((350R - 156R) / 450R) * (VREG1 - VGS) + VGS$ |
|                   | PRP/N0 6-0 = 1001111   | $((350R - 158R) / 450R) * (VREG1 - VGS) + VGS$ |
|                   | PRP/N0 6-0 = 1010000   | $((350R - 160R) / 450R) * (VREG1 - VGS) + VGS$ |
|                   | PRP/N0 6-0 = 1010001   | $((350R - 162R) / 450R) * (VREG1 - VGS) + VGS$ |
|                   | PRP/N0 6-0 = 1010010   | $((350R - 164R) / 450R) * (VREG1 - VGS) + VGS$ |
|                   | PRP/N0 6-0 = 1010011   | $((350R - 166R) / 450R) * (VREG1 - VGS) + VGS$ |
|                   | PRP/N0 6-0 = 1010100   | $((350R - 168R) / 450R) * (VREG1 - VGS) + VGS$ |
|                   | PRP/N0 6-0 = 1010101   | $((350R - 170R) / 450R) * (VREG1 - VGS) + VGS$ |
|                   | PRP/N0 6-0 = 1010110   | $((350R - 172R) / 450R) * (VREG1 - VGS) + VGS$ |
|                   | PRP/N0 6-0 = 1010111   | $((350R - 174R) / 450R) * (VREG1 - VGS) + VGS$ |
|                   | PRP/N0 6-0 = 1011000   | $((350R - 176R) / 450R) * (VREG1 - VGS) + VGS$ |
|                   | PRP/N0 6-0 = 1011001   | $((350R - 178R) / 450R) * (VREG1 - VGS) + VGS$ |
|                   | PRP/N0 6-0 = 1011010   | $((350R - 180R) / 450R) * (VREG1 - VGS) + VGS$ |
|                   | PRP/N0 6-0 = 1011011   | $((350R - 182R) / 450R) * (VREG1 - VGS) + VGS$ |
|                   | PRP/N0 6-0 = 1011100   | $((350R - 184R) / 450R) * (VREG1 - VGS) + VGS$ |
|                   | PRP/N0 6-0 = 1011101   | $((350R - 186R) / 450R) * (VREG1 - VGS) + VGS$ |
|                   | PRP/N0 6-0 = 1011110   | $((350R - 188R) / 450R) * (VREG1 - VGS) + VGS$ |
|                   | PRP/N0 6-0 = 1011111   | $((350R - 190R) / 450R) * (VREG1 - VGS) + VGS$ |
|                   | PRP/N0 6-0 = 1100000   | $((350R - 192R) / 450R) * (VREG1 - VGS) + VGS$ |
|                   | PRP/N0 6-0 = 1100001   | $((350R - 194R) / 450R) * (VREG1 - VGS) + VGS$ |
|                   | PRP/N0 6-0 = 1100010   | $((350R - 196R) / 450R) * (VREG1 - VGS) + VGS$ |
|                   | PRP/N0 6-0 = 1100011   | $((350R - 198R) / 450R) * (VREG1 - VGS) + VGS$ |
|                   | PRP/N0 6-0 = 1100100   | $((350R - 200R) / 450R) * (VREG1 - VGS) + VGS$ |
|                   | PRP/N0 6-0 = 1100101   | $((350R - 202R) / 450R) * (VREG1 - VGS) + VGS$ |
|                   | PRP/N0 6-0 = 1100110   | $((350R - 204R) / 450R) * (VREG1 - VGS) + VGS$ |
|                   | PRP/N0 6-0 = 1100111   | $((350R - 206R) / 450R) * (VREG1 - VGS) + VGS$ |
|                   | PRP/N0 6-0 = 1101000   | $((350R - 208R) / 450R) * (VREG1 - VGS) + VGS$ |
|                   | PRP/N0 6-0 = 1101001   | $((350R - 210R) / 450R) * (VREG1 - VGS) + VGS$ |
|                   | PRP/N0 6-0 = 1101010   | $((350R - 212R) / 450R) * (VREG1 - VGS) + VGS$ |
|                   | PRP/N0 6-0 = 1101011   | $((350R - 214R) / 450R) * (VREG1 - VGS) + VGS$ |
|                   | PRP/N0 6-0 = 1101100   | $((350R - 216R) / 450R) * (VREG1 - VGS) + VGS$ |
|                   | PRP/N0 6-0 = 1101101   | $((350R - 218R) / 450R) * (VREG1 - VGS) + VGS$ |
|                   | PRP/N0 6-0 = 1101110   | $((350R - 220R) / 450R) * (VREG1 - VGS) + VGS$ |
|                   | PRP/N0 6-0 = 1101111   | $((350R - 223R) / 450R) * (VREG1 - VGS) + VGS$ |
|                   | PRP/N0 6-0 = 1110000   | $((350R - 224R) / 450R) * (VREG1 - VGS) + VGS$ |
|                   | PRP/N0 6-0 = 1110001   | $((350R - 226R) / 450R) * (VREG1 - VGS) + VGS$ |
|                   | PRP/N0 6-0 = 1110010   | $((350R - 228R) / 450R) * (VREG1 - VGS) + VGS$ |
|                   | PRP/N0 6-0 = 1110011   | $((350R - 230R) / 450R) * (VREG1 - VGS) + VGS$ |
|                   | PRP/N0 6-0 = 1110100   | $((350R - 232R) / 450R) * (VREG1 - VGS) + VGS$ |
|                   | PRP/N0 6-0 = 1110101   | $((350R - 234R) / 450R) * (VREG1 - VGS) + VGS$ |
|                   | PRP/N0 6-0 = 1110110   | $((350R - 236R) / 450R) * (VREG1 - VGS) + VGS$ |
|                   | PRP/N0 6-0 = 1110111   | $((350R - 238R) / 450R) * (VREG1 - VGS) + VGS$ |
|                   | PRP/N0 6-0 = 1111000   | $((350R - 240R) / 450R) * (VREG1 - VGS) + VGS$ |
|                   | PRP/N0 6-0 = 1111001   | $((350R - 243R) / 450R) * (VREG1 - VGS) + VGS$ |
|                   | PRP/N0 6-0 = 1111010   | $((350R - 244R) / 450R) * (VREG1 - VGS) + VGS$ |
|                   | PRP/N0 6-0 = 1111011   | $((350R - 246R) / 450R) * (VREG1 - VGS) + VGS$ |
|                   | PRP/N0 6-0 = 1111100   | $((350R - 248R) / 450R) * (VREG1 - VGS) + VGS$ |
|                   | PRP/N0 6-0 = 1111101   | $((350R - 250R) / 450R) * (VREG1 - VGS) + VGS$ |
|                   | PRP/N0 6-0 = 1111110   | $((350R - 252R) / 450R) * (VREG1 - VGS) + VGS$ |
|                   | PRP/N0 6-0 = 1111111   | $((350R - 254R) / 450R) * (VREG1 - VGS) + VGS$ |

Table 5.21: VinP/N4

| Reference Voltage    | Macro Adjustment Value                         | VinP/N8 Formula                               |
|----------------------|--|---|
| VinP/N8              | PRP/N1 6-0 = 0000000                           | $(354R / 450R) (VREG1 - VGS) + VGS$           |
|                      | PRP/N1 6-0 = 0000001                           | $((354R - 2R) / 450R) * (VREG1 - VGS) + VGS$  |
|                      | PRP/N1 6-0 = 0000010                           | $((354R - 4R) / 450R) * (VREG1 - VGS) + VGS$  |
|                      | PRP/N1 6-0 = 0000011                           | $((354R - 6R) / 450R) * (VREG1 - VGS) + VGS$  |
|                      | PRP/N1 6-0 = 0000100                           | $((354R - 8R) / 450R) * (VREG1 - VGS) + VGS$  |
|                      | PRP/N1 6-0 = 0000101                           | $((354R - 10R) / 450R) * (VREG1 - VGS) + VGS$ |
|                      | PRP/N1 6-0 = 0000110                           | $((354R - 12R) / 450R) * (VREG1 - VGS) + VGS$ |
|                      | PRP/N1 6-0 = 0000111                           | $((354R - 14R) / 450R) * (VREG1 - VGS) + VGS$ |
|                      | PRP/N1 6-0 = 0001000                           | $((354R - 16R) / 450R) * (VREG1 - VGS) + VGS$ |
|                      | PRP/N1 6-0 = 0001001                           | $((354R - 18R) / 450R) * (VREG1 - VGS) + VGS$ |
|                      | PRP/N1 6-0 = 0001010                           | $((354R - 20R) / 450R) * (VREG1 - VGS) + VGS$ |
|                      | PRP/N1 6-0 = 0001011                           | $((354R - 22R) / 450R) * (VREG1 - VGS) + VGS$ |
|                      | PRP/N1 6-0 = 0001100                           | $((354R - 24R) / 450R) * (VREG1 - VGS) + VGS$ |
|                      | PRP/N1 6-0 = 0001101                           | $((354R - 26R) / 450R) * (VREG1 - VGS) + VGS$ |
|                      | PRP/N1 6-0 = 0001110                           | $((354R - 28R) / 450R) * (VREG1 - VGS) + VGS$ |
|                      | PRP/N1 6-0 = 0001111                           | $((354R - 30R) / 450R) * (VREG1 - VGS) + VGS$ |
|                      | PRP/N1 6-0 = 0010000                           | $((354R - 32R) / 450R) * (VREG1 - VGS) + VGS$ |
|                      | PRP/N1 6-0 = 0010001                           | $((354R - 34R) / 450R) * (VREG1 - VGS) + VGS$ |
|                      | PRP/N1 6-0 = 0010010                           | $((354R - 36R) / 450R) * (VREG1 - VGS) + VGS$ |
|                      | PRP/N1 6-0 = 0010011                           | $((354R - 38R) / 450R) * (VREG1 - VGS) + VGS$ |
|                      | PRP/N1 6-0 = 0010100                           | $((354R - 40R) / 450R) * (VREG1 - VGS) + VGS$ |
|                      | PRP/N1 6-0 = 0010101                           | $((354R - 42R) / 450R) * (VREG1 - VGS) + VGS$ |
|                      | PRP/N1 6-0 = 0010110                           | $((354R - 44R) / 450R) * (VREG1 - VGS) + VGS$ |
|                      | PRP/N1 6-0 = 0010111                           | $((354R - 46R) / 450R) * (VREG1 - VGS) + VGS$ |
|                      | PRP/N1 6-0 = 0011000                           | $((354R - 48R) / 450R) * (VREG1 - VGS) + VGS$ |
|                      | PRP/N1 6-0 = 0011001                           | $((354R - 50R) / 450R) * (VREG1 - VGS) + VGS$ |
|                      | PRP/N1 6-0 = 0011010                           | $((354R - 52R) / 450R) * (VREG1 - VGS) + VGS$ |
|                      | PRP/N1 6-0 = 0011011                           | $((354R - 54R) / 450R) * (VREG1 - VGS) + VGS$ |
|                      | PRP/N1 6-0 = 0011100                           | $((354R - 56R) / 450R) * (VREG1 - VGS) + VGS$ |
|                      | PRP/N1 6-0 = 0011101                           | $((354R - 58R) / 450R) * (VREG1 - VGS) + VGS$ |
|                      | PRP/N1 6-0 = 0011110                           | $((354R - 60R) / 450R) * (VREG1 - VGS) + VGS$ |
|                      | PRP/N1 6-0 = 0011111                           | $((354R - 62R) / 450R) * (VREG1 - VGS) + VGS$ |
|                      | PRP/N1 6-0 = 0100000                           | $((354R - 64R) / 450R) * (VREG1 - VGS) + VGS$ |
|                      | PRP/N1 6-0 = 0100001                           | $((354R - 66R) / 450R) * (VREG1 - VGS) + VGS$ |
|                      | PRP/N1 6-0 = 0100010                           | $((354R - 68R) / 450R) * (VREG1 - VGS) + VGS$ |
|                      | PRP/N1 6-0 = 0100011                           | $((354R - 70R) / 450R) * (VREG1 - VGS) + VGS$ |
|                      | PRP/N1 6-0 = 0100100                           | $((354R - 72R) / 450R) * (VREG1 - VGS) + VGS$ |
|                      | PRP/N1 6-0 = 0100101                           | $((354R - 74R) / 450R) * (VREG1 - VGS) + VGS$ |
|                      | PRP/N1 6-0 = 0100110                           | $((354R - 76R) / 450R) * (VREG1 - VGS) + VGS$ |
|                      | PRP/N1 6-0 = 0100111                           | $((354R - 78R) / 450R) * (VREG1 - VGS) + VGS$ |
| PRP/N1 6-0 = 0101000 | $((354R - 80R) / 450R) * (VREG1 - VGS) + VGS$  |   |
| PRP/N1 6-0 = 0101001 | $((354R - 82R) / 450R) * (VREG1 - VGS) + VGS$  |   |
| PRP/N1 6-0 = 0101010 | $((354R - 84R) / 450R) * (VREG1 - VGS) + VGS$  |   |
| PRP/N1 6-0 = 0101011 | $((354R - 86R) / 450R) * (VREG1 - VGS) + VGS$  |   |
| PRP/N1 6-0 = 0101100 | $((354R - 88R) / 450R) * (VREG1 - VGS) + VGS$  |   |
| PRP/N1 6-0 = 0101101 | $((354R - 90R) / 450R) * (VREG1 - VGS) + VGS$  |   |
| PRP/N1 6-0 = 0101110 | $((354R - 92R) / 450R) * (VREG1 - VGS) + VGS$  |   |
| PRP/N1 6-0 = 0101111 | $((354R - 94R) / 450R) * (VREG1 - VGS) + VGS$  |   |
| PRP/N1 6-0 = 0110000 | $((354R - 96R) / 450R) * (VREG1 - VGS) + VGS$  |   |
| PRP/N1 6-0 = 0110001 | $((354R - 98R) / 450R) * (VREG1 - VGS) + VGS$  |   |
| PRP/N1 6-0 = 0110010 | $((354R - 100R) / 450R) * (VREG1 - VGS) + VGS$ |   |
| PRP/N1 6-0 = 0110011 | $((354R - 102R) / 450R) * (VREG1 - VGS) + VGS$ |   |
| PRP/N1 6-0 = 0110100 | $((354R - 104R) / 450R) * (VREG1 - VGS) + VGS$ |   |
| PRP/N1 6-0 = 0110101 | $((354R - 106R) / 450R) * (VREG1 - VGS) + VGS$ |   |
| PRP/N1 6-0 = 0110110 | $((354R - 108R) / 450R) * (VREG1 - VGS) + VGS$ |   |
| PRP/N1 6-0 = 0110111 | $((354R - 110R) / 450R) * (VREG1 - VGS) + VGS$ |   |
| PRP/N1 6-0 = 0111000 | $((354R - 112R) / 450R) * (VREG1 - VGS) + VGS$ |   |
| PRP/N1 6-0 = 0111001 | $((354R - 114R) / 450R) * (VREG1 - VGS) + VGS$ |   |
| PRP/N1 6-0 = 0111010 | $((354R - 116R) / 450R) * (VREG1 - VGS) + VGS$ |   |
| PRP/N1 6-0 = 0111011 | $((354R - 118R) / 450R) * (VREG1 - VGS) + VGS$ |   |
| PRP/N1 6-0 = 0111100 | $((354R - 120R) / 450R) * (VREG1 - VGS) + VGS$ |   |
| PRP/N1 6-0 = 0111101 | $((354R - 122R) / 450R) * (VREG1 - VGS) + VGS$ |   |
| PRP/N1 6-0 = 0111110 | $((354R - 124R) / 450R) * (VREG1 - VGS) + VGS$ |   |
| PRP/N1 6-0 = 0111111 | $((354R - 126R) / 450R) * (VREG1 - VGS) + VGS$ |   |
| PRP/N1 6-0 = 1000000 | $((354R - 128R) / 450R) * (VREG1 - VGS) + VGS$ |   |
| PRP/N1 6-0 = 1000001 | $((354R - 130R) / 450R) * (VREG1 - VGS) + VGS$ |   |
| PRP/N1 6-0 = 1000010 | $((354R - 132R) / 450R) * (VREG1 - VGS) + VGS$ |   |
| PRP/N1 6-0 = 1000011 | $((354R - 134R) / 450R) * (VREG1 - VGS) + VGS$ |   |
| PRP/N1 6-0 = 1000100 | $((354R - 136R) / 450R) * (VREG1 - VGS) + VGS$ |   |

| Reference Voltage | Macro Adjustment Value | VinP/N8 Formula                                |
|-------------------|------------------------|--|
|                   | PRP/N1 6-0 = 1000101   | $((354R - 138R) / 450R) * (VREG1 - VGS) + VGS$ |
|                   | PRP/N1 6-0 = 1000110   | $((354R - 140R) / 450R) * (VREG1 - VGS) + VGS$ |
|                   | PRP/N1 6-0 = 1000111   | $((354R - 142R) / 450R) * (VREG1 - VGS) + VGS$ |
|                   | PRP/N1 6-0 = 1001000   | $((354R - 144R) / 450R) * (VREG1 - VGS) + VGS$ |
|                   | PRP/N1 6-0 = 1001001   | $((354R - 146R) / 450R) * (VREG1 - VGS) + VGS$ |
|                   | PRP/N1 6-0 = 1001010   | $((354R - 148R) / 450R) * (VREG1 - VGS) + VGS$ |
|                   | PRP/N1 6-0 = 1001011   | $((354R - 150R) / 450R) * (VREG1 - VGS) + VGS$ |
|                   | PRP/N1 6-0 = 1001100   | $((354R - 152R) / 450R) * (VREG1 - VGS) + VGS$ |
|                   | PRP/N1 6-0 = 1001101   | $((354R - 154R) / 450R) * (VREG1 - VGS) + VGS$ |
|                   | PRP/N1 6-0 = 1001110   | $((354R - 156R) / 450R) * (VREG1 - VGS) + VGS$ |
|                   | PRP/N1 6-0 = 1001111   | $((354R - 158R) / 450R) * (VREG1 - VGS) + VGS$ |
|                   | PRP/N1 6-0 = 1010000   | $((354R - 160R) / 450R) * (VREG1 - VGS) + VGS$ |
|                   | PRP/N1 6-0 = 1010001   | $((354R - 162R) / 450R) * (VREG1 - VGS) + VGS$ |
|                   | PRP/N1 6-0 = 1010010   | $((354R - 164R) / 450R) * (VREG1 - VGS) + VGS$ |
|                   | PRP/N1 6-0 = 1010011   | $((354R - 166R) / 450R) * (VREG1 - VGS) + VGS$ |
|                   | PRP/N1 6-0 = 1010100   | $((354R - 168R) / 450R) * (VREG1 - VGS) + VGS$ |
|                   | PRP/N1 6-0 = 1010101   | $((354R - 170R) / 450R) * (VREG1 - VGS) + VGS$ |
|                   | PRP/N1 6-0 = 1010110   | $((354R - 172R) / 450R) * (VREG1 - VGS) + VGS$ |
|                   | PRP/N1 6-0 = 1010111   | $((354R - 174R) / 450R) * (VREG1 - VGS) + VGS$ |
|                   | PRP/N1 6-0 = 1011000   | $((354R - 176R) / 450R) * (VREG1 - VGS) + VGS$ |
|                   | PRP/N1 6-0 = 1011001   | $((354R - 178R) / 450R) * (VREG1 - VGS) + VGS$ |
|                   | PRP/N1 6-0 = 1011010   | $((354R - 180R) / 450R) * (VREG1 - VGS) + VGS$ |
|                   | PRP/N1 6-0 = 1011011   | $((354R - 182R) / 450R) * (VREG1 - VGS) + VGS$ |
|                   | PRP/N1 6-0 = 1011100   | $((354R - 184R) / 450R) * (VREG1 - VGS) + VGS$ |
|                   | PRP/N1 6-0 = 1011101   | $((354R - 186R) / 450R) * (VREG1 - VGS) + VGS$ |
|                   | PRP/N1 6-0 = 1011110   | $((354R - 188R) / 450R) * (VREG1 - VGS) + VGS$ |
|                   | PRP/N1 6-0 = 1011111   | $((354R - 190R) / 450R) * (VREG1 - VGS) + VGS$ |
|                   | PRP/N1 6-0 = 1100000   | $((354R - 192R) / 450R) * (VREG1 - VGS) + VGS$ |
|                   | PRP/N1 6-0 = 1100001   | $((354R - 194R) / 450R) * (VREG1 - VGS) + VGS$ |
|                   | PRP/N1 6-0 = 1100010   | $((354R - 196R) / 450R) * (VREG1 - VGS) + VGS$ |
|                   | PRP/N1 6-0 = 1100011   | $((354R - 198R) / 450R) * (VREG1 - VGS) + VGS$ |
|                   | PRP/N1 6-0 = 1100100   | $((354R - 200R) / 450R) * (VREG1 - VGS) + VGS$ |
|                   | PRP/N1 6-0 = 1100101   | $((354R - 202R) / 450R) * (VREG1 - VGS) + VGS$ |
|                   | PRP/N1 6-0 = 1100110   | $((354R - 204R) / 450R) * (VREG1 - VGS) + VGS$ |
|                   | PRP/N1 6-0 = 1100111   | $((354R - 206R) / 450R) * (VREG1 - VGS) + VGS$ |
|                   | PRP/N1 6-0 = 1101000   | $((354R - 208R) / 450R) * (VREG1 - VGS) + VGS$ |
|                   | PRP/N1 6-0 = 1101001   | $((354R - 210R) / 450R) * (VREG1 - VGS) + VGS$ |
|                   | PRP/N1 6-0 = 1101010   | $((354R - 212R) / 450R) * (VREG1 - VGS) + VGS$ |
|                   | PRP/N1 6-0 = 1101011   | $((354R - 214R) / 450R) * (VREG1 - VGS) + VGS$ |
|                   | PRP/N1 6-0 = 1101100   | $((354R - 216R) / 450R) * (VREG1 - VGS) + VGS$ |
|                   | PRP/N1 6-0 = 1101101   | $((354R - 218R) / 450R) * (VREG1 - VGS) + VGS$ |
|                   | PRP/N1 6-0 = 1101110   | $((354R - 220R) / 450R) * (VREG1 - VGS) + VGS$ |
|                   | PRP/N1 6-0 = 1101111   | $((354R - 222R) / 450R) * (VREG1 - VGS) + VGS$ |
|                   | PRP/N1 6-0 = 1110000   | $((354R - 224R) / 450R) * (VREG1 - VGS) + VGS$ |
|                   | PRP/N1 6-0 = 1110001   | $((354R - 226R) / 450R) * (VREG1 - VGS) + VGS$ |
|                   | PRP/N1 6-0 = 1110010   | $((354R - 228R) / 450R) * (VREG1 - VGS) + VGS$ |
|                   | PRP/N1 6-0 = 1110011   | $((354R - 230R) / 450R) * (VREG1 - VGS) + VGS$ |
|                   | PRP/N1 6-0 = 1110100   | $((354R - 232R) / 450R) * (VREG1 - VGS) + VGS$ |
|                   | PRP/N1 6-0 = 1110101   | $((354R - 234R) / 450R) * (VREG1 - VGS) + VGS$ |
|                   | PRP/N1 6-0 = 1110110   | $((354R - 236R) / 450R) * (VREG1 - VGS) + VGS$ |
|                   | PRP/N1 6-0 = 1110111   | $((354R - 238R) / 450R) * (VREG1 - VGS) + VGS$ |
|                   | PRP/N1 6-0 = 1111000   | $((354R - 240R) / 450R) * (VREG1 - VGS) + VGS$ |
|                   | PRP/N1 6-0 = 1111001   | $((354R - 242R) / 450R) * (VREG1 - VGS) + VGS$ |
|                   | PRP/N1 6-0 = 1111010   | $((354R - 244R) / 450R) * (VREG1 - VGS) + VGS$ |
|                   | PRP/N1 6-0 = 1111011   | $((354R - 246R) / 450R) * (VREG1 - VGS) + VGS$ |
|                   | PRP/N1 6-0 = 1111100   | $((354R - 248R) / 450R) * (VREG1 - VGS) + VGS$ |
|                   | PRP/N1 6-0 = 1111101   | $((354R - 250R) / 450R) * (VREG1 - VGS) + VGS$ |
|                   | PRP/N1 6-0 = 1111110   | $((354R - 252R) / 450R) * (VREG1 - VGS) + VGS$ |
|                   | PRP/N1 6-0 = 1111111   | $((354R - 254R) / 450R) * (VREG1 - VGS) + VGS$ |

Table 5.22: VinP/N 8



| Reference Voltage  | Macro Adjustment Value                                | VinP/N3 Formula                                       |
|--------------------|---|---|
| VinP/N3            | PKP/N0 4-0 = 00000                                    | $(31R / 32R) * (VinP/N2 - VinP/N4) + VinP/N4$         |
|                    | PKP/N0 4-0 = 00001                                    | $((31R - 1R) / 32R) * (VinP/N2 - VinP/N4) + VinP/N4$  |
|                    | PKP/N0 4-0 = 00010                                    | $((31R - 2R) / 32R) * (VinP/N2 - VinP/N4) + VinP/N4$  |
|                    | PKP/N0 4-0 = 00011                                    | $((31R - 3R) / 32R) * (VinP/N2 - VinP/N4) + VinP/N4$  |
|                    | PKP/N0 4-0 = 00100                                    | $((31R - 4R) / 32R) * (VinP/N2 - VinP/N4) + VinP/N4$  |
|                    | PKP/N0 4-0 = 00101                                    | $((31R - 5R) / 32R) * (VinP/N2 - VinP/N4) + VinP/N4$  |
|                    | PKP/N0 4-0 = 00110                                    | $((31R - 6R) / 32R) * (VinP/N2 - VinP/N4) + VinP/N4$  |
|                    | PKP/N0 4-0 = 00111                                    | $((31R - 7R) / 32R) * (VinP/N2 - VinP/N4) + VinP/N4$  |
|                    | PKP/N0 4-0 = 01000                                    | $((31R - 8R) / 32R) * (VinP/N2 - VinP/N4) + VinP/N4$  |
|                    | PKP/N0 4-0 = 01001                                    | $((31R - 9R) / 32R) * (VinP/N2 - VinP/N4) + VinP/N4$  |
|                    | PKP/N0 4-0 = 01010                                    | $((31R - 10R) / 32R) * (VinP/N2 - VinP/N4) + VinP/N4$ |
|                    | PKP/N0 4-0 = 01011                                    | $((31R - 11R) / 32R) * (VinP/N2 - VinP/N4) + VinP/N4$ |
|                    | PKP/N0 4-0 = 01100                                    | $((31R - 12R) / 32R) * (VinP/N2 - VinP/N4) + VinP/N4$ |
|                    | PKP/N0 4-0 = 01101                                    | $((31R - 13R) / 32R) * (VinP/N2 - VinP/N4) + VinP/N4$ |
|                    | PKP/N0 4-0 = 01110                                    | $((31R - 14R) / 32R) * (VinP/N2 - VinP/N4) + VinP/N4$ |
|                    | PKP/N0 4-0 = 01111                                    | $((31R - 15R) / 32R) * (VinP/N2 - VinP/N4) + VinP/N4$ |
|                    | PKP/N0 4-0 = 10000                                    | $((31R - 16R) / 32R) * (VinP/N2 - VinP/N4) + VinP/N4$ |
|                    | PKP/N0 4-0 = 10001                                    | $((31R - 17R) / 32R) * (VinP/N2 - VinP/N4) + VinP/N4$ |
|                    | PKP/N0 4-0 = 10010                                    | $((31R - 18R) / 32R) * (VinP/N2 - VinP/N4) + VinP/N4$ |
|                    | PKP/N0 4-0 = 10011                                    | $((31R - 19R) / 32R) * (VinP/N2 - VinP/N4) + VinP/N4$ |
|                    | PKP/N0 4-0 = 10100                                    | $((31R - 20R) / 32R) * (VinP/N2 - VinP/N4) + VinP/N4$ |
|                    | PKP/N0 4-0 = 10101                                    | $((31R - 21R) / 32R) * (VinP/N2 - VinP/N4) + VinP/N4$ |
|                    | PKP/N0 4-0 = 10110                                    | $((31R - 22R) / 32R) * (VinP/N2 - VinP/N4) + VinP/N4$ |
|                    | PKP/N0 4-0 = 10111                                    | $((31R - 23R) / 32R) * (VinP/N2 - VinP/N4) + VinP/N4$ |
|                    | PKP/N0 4-0 = 11000                                    | $((31R - 24R) / 32R) * (VinP/N2 - VinP/N4) + VinP/N4$ |
|                    | PKP/N0 4-0 = 11001                                    | $((31R - 25R) / 32R) * (VinP/N2 - VinP/N4) + VinP/N4$ |
|                    | PKP/N0 4-0 = 11010                                    | $((31R - 26R) / 32R) * (VinP/N2 - VinP/N4) + VinP/N4$ |
|                    | PKP/N0 4-0 = 11011                                    | $((31R - 27R) / 32R) * (VinP/N2 - VinP/N4) + VinP/N4$ |
|                    | PKP/N0 4-0 = 11100                                    | $((31R - 28R) / 32R) * (VinP/N2 - VinP/N4) + VinP/N4$ |
|                    | PKP/N0 4-0 = 11101                                    | $((31R - 29R) / 32R) * (VinP/N2 - VinP/N4) + VinP/N4$ |
| PKP/N0 4-0 = 11110 | $((31R - 30R) / 32R) * (VinP/N2 - VinP/N4) + VinP/N4$ |   |
| PKP/N0 4-0 = 11111 | $((31R - 31R) / 32R) * (VinP/N2 - VinP/N4) + VinP/N4$ |   |

Table 5.23: VinP/N 3

| Reference Voltage  | Macro Adjustment Value                                  | VinP/N5 Formula   |
|--------------------|---|---|
| VinP/N5            | PKP/N1 4-0 = 00000                                      | $(193R / 223R) * (VinP/N4 - VinP/N8) + VinP/N8$         |
|                    | PKP/N1 4-0 = 00001                                      | $((193R - 3R) / 223R) * (VinP/N4 - VinP/N8) + VinP/N8$  |
|                    | PKP/N1 4-0 = 00010                                      | $((193R - 6R) / 223R) * (VinP/N4 - VinP/N8) + VinP/N8$  |
|                    | PKP/N1 4-0 = 00011                                      | $((193R - 9R) / 223R) * (VinP/N4 - VinP/N8) + VinP/N8$  |
|                    | PKP/N14-0 = 00100                                       | $((193R - 12R) / 223R) * (VinP/N4 - VinP/N8) + VinP/N8$ |
|                    | PKP/N1 4-0 = 00101                                      | $((193R - 15R) / 223R) * (VinP/N4 - VinP/N8) + VinP/N8$ |
|                    | PKP/N1 4-0 = 00110                                      | $((193R - 18R) / 223R) * (VinP/N4 - VinP/N8) + VinP/N8$ |
|                    | PKP/N1 4-0 = 00111                                      | $((193R - 21R) / 223R) * (VinP/N4 - VinP/N8) + VinP/N8$ |
|                    | PKP/N1 4-0 = 01000                                      | $((193R - 24R) / 223R) * (VinP/N4 - VinP/N8) + VinP/N8$ |
|                    | PKP/N1 4-0 = 01001                                      | $((193R - 27R) / 223R) * (VinP/N4 - VinP/N8) + VinP/N8$ |
|                    | PKP/N1 4-0 = 01010                                      | $((193R - 30R) / 223R) * (VinP/N4 - VinP/N8) + VinP/N8$ |
|                    | PKP/N1 4-0 = 01011                                      | $((193R - 33R) / 223R) * (VinP/N4 - VinP/N8) + VinP/N8$ |
|                    | PKP/N1 4-0 = 01100                                      | $((193R - 36R) / 223R) * (VinP/N4 - VinP/N8) + VinP/N8$ |
|                    | PKP/N1 4-0 = 01101                                      | $((193R - 39R) / 223R) * (VinP/N4 - VinP/N8) + VinP/N8$ |
|                    | PKP/N1 4-0 = 01110                                      | $((193R - 42R) / 223R) * (VinP/N4 - VinP/N8) + VinP/N8$ |
|                    | PKP/N1 4-0 = 01111                                      | $((193R - 45R) / 223R) * (VinP/N4 - VinP/N8) + VinP/N8$ |
|                    | PKP/N1 4-0 = 10000                                      | $((193R - 48R) / 223R) * (VinP/N4 - VinP/N8) + VinP/N8$ |
|                    | PKP/N1 4-0 = 10001                                      | $((193R - 51R) / 223R) * (VinP/N4 - VinP/N8) + VinP/N8$ |
|                    | PKP/N1 4-0 = 10010                                      | $((193R - 54R) / 223R) * (VinP/N4 - VinP/N8) + VinP/N8$ |
|                    | PKP/N1 4-0 = 10011                                      | $((193R - 57R) / 223R) * (VinP/N4 - VinP/N8) + VinP/N8$ |
|                    | PKP/N1 4-0 = 10100                                      | $((193R - 60R) / 223R) * (VinP/N4 - VinP/N8) + VinP/N8$ |
|                    | PKP/N1 4-0 = 10101                                      | $((193R - 63R) / 223R) * (VinP/N4 - VinP/N8) + VinP/N8$ |
|                    | PKP/N1 4-0 = 10110                                      | $((193R - 66R) / 223R) * (VinP/N4 - VinP/N8) + VinP/N8$ |
|                    | PKP/N1 4-0 = 10111                                      | $((193R - 69R) / 223R) * (VinP/N4 - VinP/N8) + VinP/N8$ |
|                    | PKP/N1 4-0 = 11000                                      | $((193R - 72R) / 223R) * (VinP/N4 - VinP/N8) + VinP/N8$ |
|                    | PKP/N1 4-0 = 11001                                      | $((193R - 75R) / 223R) * (VinP/N4 - VinP/N8) + VinP/N8$ |
|                    | PKP/N1 4-0 = 11010                                      | $((193R - 78R) / 223R) * (VinP/N4 - VinP/N8) + VinP/N8$ |
|                    | PKP/N1 4-0 = 11011                                      | $((193R - 81R) / 223R) * (VinP/N4 - VinP/N8) + VinP/N8$ |
|                    | PKP/N1 4-0 = 11100                                      | $((193R - 84R) / 223R) * (VinP/N4 - VinP/N8) + VinP/N8$ |
|                    | PKP/N1 4-0 = 11101                                      | $((193R - 87R) / 223R) * (VinP/N4 - VinP/N8) + VinP/N8$ |
| PKP/N1 4-0 = 11110 | $((193R - 90R) / 223R) * (VinP/N4 - VinP/N8) + VinP/N8$ |   |
| PKP/N1 4-0 = 11111 | $((193R - 93R) / 223R) * (VinP/N4 - VinP/N8) + VinP/N8$ |   |

Table 5.24: VinP/N 5

| Reference Voltage  | Macro Adjustment Value                                  | VinP/N6 Formula   |
|--------------------|---|---|
| VinP/N6            | PKP/N2 4-0 = 00000                                      | $(158R / 223R) * (VinP/N4 - VinP/N8) + VinP/N8$         |
|                    | PKP/N2 4-0 = 00001                                      | $((158R - 3R) / 223R) * (VinP/N4 - VinP/N8) + VinP/N8$  |
|                    | PKP/N2 4-0 = 00010                                      | $((158R - 6R) / 223R) * (VinP/N4 - VinP/N8) + VinP/N8$  |
|                    | PKP/N2 4-0 = 00011                                      | $((158R - 9R) / 223R) * (VinP/N4 - VinP/N8) + VinP/N8$  |
|                    | PKP/N2 4-0 = 00100                                      | $((158R - 12R) / 223R) * (VinP/N4 - VinP/N8) + VinP/N8$ |
|                    | PKP/N2 4-0 = 00101                                      | $((158R - 15R) / 223R) * (VinP/N4 - VinP/N8) + VinP/N8$ |
|                    | PKP/N2 4-0 = 00110                                      | $((158R - 18R) / 223R) * (VinP/N4 - VinP/N8) + VinP/N8$ |
|                    | PKP/N2 4-0 = 00111                                      | $((158R - 21R) / 223R) * (VinP/N4 - VinP/N8) + VinP/N8$ |
|                    | PKP/N2 4-0 = 01000                                      | $((158R - 24R) / 223R) * (VinP/N4 - VinP/N8) + VinP/N8$ |
|                    | PKP/N2 4-0 = 01001                                      | $((158R - 27R) / 223R) * (VinP/N4 - VinP/N8) + VinP/N8$ |
|                    | PKP/N2 4-0 = 01010                                      | $((158R - 30R) / 223R) * (VinP/N4 - VinP/N8) + VinP/N8$ |
|                    | PKP/N2 4-0 = 01011                                      | $((158R - 33R) / 223R) * (VinP/N4 - VinP/N8) + VinP/N8$ |
|                    | PKP/N2 4-0 = 01100                                      | $((158R - 36R) / 223R) * (VinP/N4 - VinP/N8) + VinP/N8$ |
|                    | PKP/N2 4-0 = 01101                                      | $((158R - 39R) / 223R) * (VinP/N4 - VinP/N8) + VinP/N8$ |
|                    | PKP/N2 4-0 = 01110                                      | $((158R - 42R) / 223R) * (VinP/N4 - VinP/N8) + VinP/N8$ |
|                    | PKP/N2 4-0 = 01111                                      | $((158R - 45R) / 223R) * (VinP/N4 - VinP/N8) + VinP/N8$ |
|                    | PKP/N2 4-0 = 10000                                      | $((158R - 48R) / 223R) * (VinP/N4 - VinP/N8) + VinP/N8$ |
|                    | PKP/N2 4-0 = 10001                                      | $((158R - 51R) / 223R) * (VinP/N4 - VinP/N8) + VinP/N8$ |
|                    | PKP/N2 4-0 = 10010                                      | $((158R - 54R) / 223R) * (VinP/N4 - VinP/N8) + VinP/N8$ |
|                    | PKP/N2 4-0 = 10011                                      | $((158R - 57R) / 223R) * (VinP/N4 - VinP/N8) + VinP/N8$ |
|                    | PKP/N2 4-0 = 10100                                      | $((158R - 60R) / 223R) * (VinP/N4 - VinP/N8) + VinP/N8$ |
|                    | PKP/N2 4-0 = 10101                                      | $((158R - 63R) / 223R) * (VinP/N4 - VinP/N8) + VinP/N8$ |
|                    | PKP/N2 4-0 = 10110                                      | $((158R - 66R) / 223R) * (VinP/N4 - VinP/N8) + VinP/N8$ |
|                    | PKP/N2 4-0 = 10111                                      | $((158R - 69R) / 223R) * (VinP/N4 - VinP/N8) + VinP/N8$ |
|                    | PKP/N2 4-0 = 11000                                      | $((158R - 72R) / 223R) * (VinP/N4 - VinP/N8) + VinP/N8$ |
|                    | PKP/N2 4-0 = 11001                                      | $((158R - 75R) / 223R) * (VinP/N4 - VinP/N8) + VinP/N8$ |
|                    | PKP/N2 4-0 = 11010                                      | $((158R - 78R) / 223R) * (VinP/N4 - VinP/N8) + VinP/N8$ |
|                    | PKP/N2 4-0 = 11011                                      | $((158R - 81R) / 223R) * (VinP/N4 - VinP/N8) + VinP/N8$ |
|                    | PKP/N2 4-0 = 11100                                      | $((158R - 84R) / 223R) * (VinP/N4 - VinP/N8) + VinP/N8$ |
|                    | PKP/N2 4-0 = 11101                                      | $((158R - 87R) / 223R) * (VinP/N4 - VinP/N8) + VinP/N8$ |
| PKP/N2 4-0 = 11110 | $((158R - 90R) / 223R) * (VinP/N4 - VinP/N8) + VinP/N8$ |   |
| PKP/N2 4-0 = 11111 | $((158R - 93R) / 223R) * (VinP/N4 - VinP/N8) + VinP/N8$ |   |

Table 5.25: VinP/N 6

| Reference Voltage  | Macro Adjustment Value                                  | VinP/N7 Formula   |
|--------------------|---|---|
| VinP/N7            | PKP/N3 4-0 = 00000                                      | $(123R / 223R) * (VinP/N4 - VinP/N8) + VinP/N8$         |
|                    | PKP/N3 4-0 = 00001                                      | $((123R - 3R) / 223R) * (VinP/N4 - VinP/N8) + VinP/N8$  |
|                    | PKP/N3 4-0 = 00010                                      | $((123R - 6R) / 223R) * (VinP/N4 - VinP/N8) + VinP/N8$  |
|                    | PKP/N3 4-0 = 00011                                      | $((123R - 9R) / 223R) * (VinP/N4 - VinP/N8) + VinP/N8$  |
|                    | PKP/N3 4-0 = 00100                                      | $((123R - 12R) / 223R) * (VinP/N4 - VinP/N8) + VinP/N8$ |
|                    | PKP/N3 4-0 = 00101                                      | $((123R - 15R) / 223R) * (VinP/N4 - VinP/N8) + VinP/N8$ |
|                    | PKP/N3 4-0 = 00110                                      | $((123R - 18R) / 223R) * (VinP/N4 - VinP/N8) + VinP/N8$ |
|                    | PKP/N3 4-0 = 00111                                      | $((123R - 21R) / 223R) * (VinP/N4 - VinP/N8) + VinP/N8$ |
|                    | PKP/N3 4-0 = 01000                                      | $((123R - 24R) / 223R) * (VinP/N4 - VinP/N8) + VinP/N8$ |
|                    | PKP/N3 4-0 = 01001                                      | $((123R - 27R) / 223R) * (VinP/N4 - VinP/N8) + VinP/N8$ |
|                    | PKP/N3 4-0 = 01010                                      | $((123R - 30R) / 223R) * (VinP/N4 - VinP/N8) + VinP/N8$ |
|                    | PKP/N3 4-0 = 01011                                      | $((123R - 33R) / 223R) * (VinP/N4 - VinP/N8) + VinP/N8$ |
|                    | PKP/N3 4-0 = 01100                                      | $((123R - 36R) / 223R) * (VinP/N4 - VinP/N8) + VinP/N8$ |
|                    | PKP/N3 4-0 = 01101                                      | $((123R - 39R) / 223R) * (VinP/N4 - VinP/N8) + VinP/N8$ |
|                    | PKP/N3 4-0 = 01110                                      | $((123R - 42R) / 223R) * (VinP/N4 - VinP/N8) + VinP/N8$ |
|                    | PKP/N3 4-0 = 01111                                      | $((123R - 45R) / 223R) * (VinP/N4 - VinP/N8) + VinP/N8$ |
|                    | PKP/N3 4-0 = 10000                                      | $((123R - 48R) / 223R) * (VinP/N4 - VinP/N8) + VinP/N8$ |
|                    | PKP/N3 4-0 = 10001                                      | $((123R - 51R) / 223R) * (VinP/N4 - VinP/N8) + VinP/N8$ |
|                    | PKP/N3 4-0 = 10010                                      | $((123R - 54R) / 223R) * (VinP/N4 - VinP/N8) + VinP/N8$ |
|                    | PKP/N3 4-0 = 10011                                      | $((123R - 57R) / 223R) * (VinP/N4 - VinP/N8) + VinP/N8$ |
|                    | PKP/N3 4-0 = 10100                                      | $((123R - 60R) / 223R) * (VinP/N4 - VinP/N8) + VinP/N8$ |
|                    | PKP/N3 4-0 = 10101                                      | $((123R - 63R) / 223R) * (VinP/N4 - VinP/N8) + VinP/N8$ |
|                    | PKP/N3 4-0 = 10110                                      | $((123R - 66R) / 223R) * (VinP/N4 - VinP/N8) + VinP/N8$ |
|                    | PKP/N3 4-0 = 10111                                      | $((123R - 69R) / 223R) * (VinP/N4 - VinP/N8) + VinP/N8$ |
|                    | PKP/N3 4-0 = 11000                                      | $((123R - 72R) / 223R) * (VinP/N4 - VinP/N8) + VinP/N8$ |
|                    | PKP/N3 4-0 = 11001                                      | $((123R - 75R) / 223R) * (VinP/N4 - VinP/N8) + VinP/N8$ |
|                    | PKP/N3 4-0 = 11010                                      | $((123R - 78R) / 223R) * (VinP/N4 - VinP/N8) + VinP/N8$ |
|                    | PKP/N3 4-0 = 11011                                      | $((123R - 81R) / 223R) * (VinP/N4 - VinP/N8) + VinP/N8$ |
|                    | PKP/N3 4-0 = 11100                                      | $((123R - 84R) / 223R) * (VinP/N4 - VinP/N8) + VinP/N8$ |
|                    | PKP/N3 4-0 = 11101                                      | $((123R - 87R) / 223R) * (VinP/N4 - VinP/N8) + VinP/N8$ |
| PKP/N3 4-0 = 11110 | $((123R - 90R) / 223R) * (VinP/N4 - VinP/N8) + VinP/N8$ |   |
| PKP/N3 4-0 = 11111 | $((123R - 93R) / 223R) * (VinP/N4 - VinP/N8) + VinP/N8$ |   |

Table 5.26: VinP/N 7

| Reference Voltage | Macro Adjustment Value | VinP/N9 Formula   |
|-------------------|------------------------|---|
| VinP/N9           | PKP/N4 4-0 = 00000     | $(31R / 32R) * (VinP/N8 - VinP/N10) + VinP/N10$         |
|                   | PKP/N4 4-0 = 00001     | $((31R - 1R) / 32R) * (VinP/N8 - VinP/N10) + VinP/N10$  |
|                   | PKP/N4 4-0 = 00010     | $((31R - 2R) / 32R) * (VinP/N8 - VinP/N10) + VinP/N10$  |
|                   | PKP/N4 4-0 = 00011     | $((31R - 3R) / 32R) * (VinP/N8 - VinP/N10) + VinP/N10$  |
|                   | PKP/N4 4-0 = 00100     | $((31R - 4R) / 32R) * (VinP/N8 - VinP/N10) + VinP/N10$  |
|                   | PKP/N4 4-0 = 00101     | $((31R - 5R) / 32R) * (VinP/N8 - VinP/N10) + VinP/N10$  |
|                   | PKP/N4 4-0 = 00110     | $((31R - 6R) / 32R) * (VinP/N8 - VinP/N10) + VinP/N10$  |
|                   | PKP/N4 4-0 = 00111     | $((31R - 7R) / 32R) * (VinP/N8 - VinP/N10) + VinP/N10$  |
|                   | PKP/N4 4-0 = 01000     | $((31R - 8R) / 32R) * (VinP/N8 - VinP/N10) + VinP/N10$  |
|                   | PKP/N4 4-0 = 01001     | $((31R - 9R) / 32R) * (VinP/N8 - VinP/N10) + VinP/N10$  |
|                   | PKP/N4 4-0 = 01010     | $((31R - 10R) / 32R) * (VinP/N8 - VinP/N10) + VinP/N10$ |
|                   | PKP/N4 4-0 = 01011     | $((31R - 11R) / 32R) * (VinP/N8 - VinP/N10) + VinP/N10$ |
|                   | PKP/N4 4-0 = 01100     | $((31R - 12R) / 32R) * (VinP/N8 - VinP/N10) + VinP/N10$ |
|                   | PKP/N4 4-0 = 01101     | $((31R - 13R) / 32R) * (VinP/N8 - VinP/N10) + VinP/N10$ |
|                   | PKP/N4 4-0 = 01110     | $((31R - 14R) / 32R) * (VinP/N8 - VinP/N10) + VinP/N10$ |
|                   | PKP/N4 4-0 = 01111     | $((31R - 15R) / 32R) * (VinP/N8 - VinP/N10) + VinP/N10$ |
|                   | PKP/N4 4-0 = 10000     | $((31R - 16R) / 32R) * (VinP/N8 - VinP/N10) + VinP/N10$ |
|                   | PKP/N4 4-0 = 10001     | $((31R - 17R) / 32R) * (VinP/N8 - VinP/N10) + VinP/N10$ |
|                   | PKP/N4 4-0 = 10010     | $((31R - 18R) / 32R) * (VinP/N8 - VinP/N10) + VinP/N10$ |
|                   | PKP/N4 4-0 = 10011     | $((31R - 19R) / 32R) * (VinP/N8 - VinP/N10) + VinP/N10$ |
|                   | PKP/N4 4-0 = 10100     | $((31R - 20R) / 32R) * (VinP/N8 - VinP/N10) + VinP/N10$ |
|                   | PKP/N4 4-0 = 10101     | $((31R - 21R) / 32R) * (VinP/N8 - VinP/N10) + VinP/N10$ |
|                   | PKP/N4 4-0 = 10110     | $((31R - 22R) / 32R) * (VinP/N8 - VinP/N10) + VinP/N10$ |
|                   | PKP/N4 4-0 = 10111     | $((31R - 23R) / 32R) * (VinP/N8 - VinP/N10) + VinP/N10$ |
|                   | PKP/N4 4-0 = 11000     | $((31R - 24R) / 32R) * (VinP/N8 - VinP/N10) + VinP/N10$ |
|                   | PKP/N4 4-0 = 11001     | $((31R - 25R) / 32R) * (VinP/N8 - VinP/N10) + VinP/N10$ |
|                   | PKP/N4 4-0 = 11010     | $((31R - 26R) / 32R) * (VinP/N8 - VinP/N10) + VinP/N10$ |
|                   | PKP/N4 4-0 = 11011     | $((31R - 27R) / 32R) * (VinP/N8 - VinP/N10) + VinP/N10$ |
|                   | PKP/N4 4-0 = 11100     | $((31R - 28R) / 32R) * (VinP/N8 - VinP/N10) + VinP/N10$ |
|                   | PKP/N4 4-0 = 11101     | $((31R - 29R) / 32R) * (VinP/N8 - VinP/N10) + VinP/N10$ |
|                   | PKP/N4 4-0 = 11110     | $((31R - 30R) / 32R) * (VinP/N8 - VinP/N10) + VinP/N10$ |
|                   | PKP/N4 4-0 = 11111     | $((31R - 31R) / 32R) * (VinP/N8 - VinP/N10) + VinP/N10$ |

Table 5.27: VinP/N 9

| Grayscale Voltage | Formula                        | Grayscale Voltage | Formula                        |
|-------------------|--------------------------------|-------------------|--------------------------------|
| V0                | VinP0                          | V32               | VinP6                          |
| V1                | VinP1                          | V33               | VinP7+(VinP6- VinP7)*(20R/22R) |
| V2                | VinP2                          | V34               | VinP7+(VinP6- VinP7)*(18R/22R) |
| V3                | VinP3                          | V35               | VinP7+(VinP6- VinP7)*(16R/22R) |
| V4                | VinP4+ (VinP3 - VinP4)*CT1     | V36               | VinP7+(VinP6- VinP7)*(14R/22R) |
| V5                | VinP4+ (VinP3 - VinP4)*CT2     | V37               | VinP7+(VinP6- VinP7)*(12R/22R) |
| V6                | VinP4+ (VinP3 - VinP4)*CT3     | V38               | VinP7+(VinP6- VinP7)*(10R/22R) |
| V7                | VinP4+ (VinP3 - VinP4)*CT4     | V39               | VinP7+(VinP6- VinP7)*(8R/22R)  |
| V8                | VinP4                          | V40               | VinP7+(VinP6- VinP7)*(6R/22R)  |
| V9                | VinP5+(VinP4- VinP5)*(22R/24R) | V41               | VinP7+(VinP6- VinP7)*(4R/22R)  |
| V10               | VinP5+(VinP4- VinP5)*(20R/24R) | V42               | VinP7+(VinP6- VinP7)*(2R/22R)  |
| V11               | VinP5+(VinP4- VinP5)*(18R/24R) | V43               | VinP7                          |
| V12               | VinP5+(VinP4- VinP5)*(16R/24R) | V44               | VinP8+(VinP7- VinP8)*(22R/24R) |
| V13               | VinP5+(VinP4- VinP5)*(14R/24R) | V45               | VinP8+(VinP7- VinP8)*(20R/24R) |
| V14               | VinP5+(VinP4- VinP5)*(12R/24R) | V46               | VinP8+(VinP7- VinP8)*(18R/24R) |
| V15               | VinP5+(VinP4- VinP5)*(10R/24R) | V47               | VinP8+(VinP7- VinP8)*(16R/24R) |
| V16               | VinP5+(VinP4- VinP5)*(8R/24R)  | V48               | VinP8+(VinP7- VinP8)*(14R/24R) |
| V17               | VinP5+(VinP4- VinP5)*(6R/24R)  | V49               | VinP8+(VinP7- VinP8)*(12R/24R) |
| V18               | VinP5+(VinP4- VinP5)*(4R/24R)  | V50               | VinP8+(VinP7- VinP8)*(10R/24R) |
| V19               | VinP5+(VinP4- VinP5)*(2R/24R)  | V51               | VinP8+(VinP7- VinP8)*(8R/24R)  |
| V20               | VinP5                          | V52               | VinP8+(VinP7- VinP8)*(6R/24R)  |
| V21               | VinP6+(VinP5- VinP6)*(22R/24R) | V53               | VinP8+(VinP7- VinP8)*(4R/24R)  |
| V22               | VinP6+(VinP5- VinP6)*(20R/24R) | V54               | VinP8+(VinP7- VinP8)*(2R/24R)  |
| V23               | VinP6+(VinP5- VinP6)*(18R/24R) | V55               | VinP8                          |
| V24               | VinP6+(VinP5- VinP6)*(16R/24R) | V56               | VinP9+ (VinP8 - VinP9)*CB1     |
| V25               | VinP6+(VinP5- VinP6)*(14R/24R) | V57               | VinP9+ (VinP8 - VinP9)*CB2     |
| V26               | VinP6+(VinP5- VinP6)*(12R/24R) | V58               | VinP9+ (VinP8 - VinP9)*CB3     |
| V27               | VinP6+(VinP5- VinP6)*(10R/24R) | V59               | VinP9+ (VinP8 - VinP9)*CB4     |
| V28               | VinP6+(VinP5- VinP6)*(8R/24R)  | V60               | VinP9                          |
| V29               | VinP6+(VinP5- VinP6)*(6R/24R)  | V61               | VinP10                         |
| V30               | VinP6+(VinP5- VinP6)*(4R/24R)  | V62               | VinP11                         |
| V31               | VinP6+(VinP5- VinP6)*(2R/24R)  | V63               | VinP12                         |

Table 5.28: Voltage calculation formula of 64-grayscale voltage (positive polarity)

| CGMP0[1:0] | “00” | “01”  | “10”  | “11”  | CGMP1[1:0] | “00” | “01”  | “10”  | “11”  |
|------------|------|-------|-------|-------|------------|------|-------|-------|-------|
| CT1        | 3/4  | 28/45 | 26/33 | 3/4   | CB1        | 4/5  | 18/19 | 44/47 | 17/20 |
| CT2        | 1/2  | 4/15  | 6/11  | 21/40 | CB2        | 3/5  | 50/57 | 40/47 | 27/40 |
| CT3        | 7/24 | 7/45  | 10/33 | 13/40 | CB3        | 2/5  | 15/19 | 35/47 | 19/40 |
| CT4        | 1/8  | 1/15  | 1/6   | 3/20  | CB4        | 1/5  | 23/57 | 28/47 | 1/4   |

Table 5.29: Voltage calculation formula of grayscale voltage V4~V7 and V56~V59

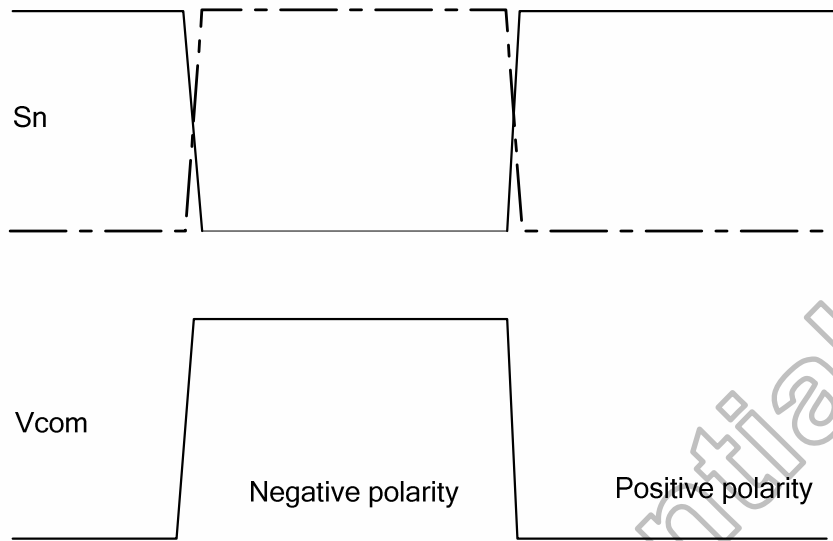
| Grayscale Voltage | Formula                          | Grayscale Voltage | Formula                          |
|-------------------|----------------------------------|-------------------|----------------------------------|
| V63               | VinN0                            | V31               | $VinN7+(VinN6- VinN7)*(22R/24R)$ |
| V62               | VinN1                            | V30               | $VinN7+(VinN6- VinN7)*(20R/24R)$ |
| V61               | VinN2                            | V29               | $VinN7+(VinN6- VinN7)*(18R/24R)$ |
| V60               | VinN3                            | V28               | $VinN7+(VinN6- VinN7)*(16R/24R)$ |
| V59               | $VinN4+(VinN3- VinN4)*CT1$       | V27               | $VinN7+(VinN6- VinN7)*(14R/24R)$ |
| V58               | $VinN4+(VinN3- VinN4)*CT2$       | V26               | $VinN7+(VinN6- VinN7)*(12R/24R)$ |
| V57               | $VinN4+(VinN3- VinN4)*CT3$       | V25               | $VinN7+(VinN6- VinN7)*(10R/24R)$ |
| V56               | $VinN4+(VinN3- VinN4)*CT4$       | V24               | $VinN7+(VinN6- VinN7)*(8R/24R)$  |
| V55               | VinN4                            | V23               | $VinN7+(VinN6- VinN7)*(6R/24R)$  |
| V54               | $VinN5+(VinN4- VinN5)*(22R/24R)$ | V22               | $VinN7+(VinN6- VinN7)*(4R/24R)$  |
| V53               | $VinN5+(VinN4- VinN5)*(20R/24R)$ | V21               | $VinN7+(VinN6- VinN7)*(2R/24R)$  |
| V52               | $VinN5+(VinN4- VinN5)*(18R/24R)$ | V20               | VinN7                            |
| V51               | $VinN5+(VinN4- VinN5)*(16R/24R)$ | V19               | $VinN8+(VinN7- VinN8)*(22R/24R)$ |
| V50               | $VinN5+(VinN4- VinN5)*(14R/24R)$ | V18               | $VinN8+(VinN7- VinN8)*(20R/24R)$ |
| V49               | $VinN5+(VinN4- VinN5)*(12R/24R)$ | V17               | $VinN8+(VinN7- VinN8)*(18R/24R)$ |
| V48               | $VinN5+(VinN4- VinN5)*(10R/24R)$ | V16               | $VinN8+(VinN7- VinN8)*(16R/24R)$ |
| V47               | $VinN5+(VinN4- VinN5)*(8R/24R)$  | V15               | $VinN8+(VinN7- VinN8)*(14R/24R)$ |
| V46               | $VinN5+(VinN4- VinN5)*(6R/24R)$  | V14               | $VinN8+(VinN7- VinN8)*(12R/24R)$ |
| V45               | $VinN5+(VinN4- VinN5)*(4R/24R)$  | V13               | $VinN8+(VinN7- VinN8)*(10R/24R)$ |
| V44               | $VinN5+(VinN4- VinN5)*(2R/24R)$  | V12               | $VinN8+(VinN7- VinN8)*(8R/24R)$  |
| V43               | VinN5                            | V11               | $VinN8+(VinN7- VinN8)*(6R/24R)$  |
| V42               | $VinN6+(VinN5- VinN6)*(20R/22R)$ | V10               | $VinN8+(VinN7- VinN8)*(4R/24R)$  |
| V41               | $VinN6+(VinN5- VinN6)*(18R/22R)$ | V9                | $VinN8+(VinN7- VinN8)*(2R/24R)$  |
| V40               | $VinN6+(VinN5- VinN6)*(16R/22R)$ | V8                | VinN8                            |
| V39               | $VinN6+(VinN5- VinN6)*(14R/22R)$ | V7                | $VinN9+(VinN8- VinN9)*CB1$       |
| V38               | $VinN6+(VinN5- VinN6)*(12R/22R)$ | V6                | $VinN9+(VinN8- VinN9)*CB2$       |
| V37               | $VinN6+(VinN5- VinN6)*(10R/22R)$ | V5                | $VinN9+(VinN8- VinN9)*CB3$       |
| V36               | $VinN6+(VinN5- VinN6)*(8R/22R)$  | V4                | $VinN9+(VinN8- VinN9)*CB4$       |
| V35               | $VinN6+(VinN5- VinN6)*(6R/22R)$  | V3                | VinN9                            |
| V34               | $VinN6+(VinN5- VinN6)*(4R/22R)$  | V2                | VinN10                           |
| V33               | $VinN6+(VinN5- VinN6)*(2R/22R)$  | V1                | VinN11                           |
| V32               | VinN6                            | V0                | VinN12                           |

Table 5.30: Voltage calculation formula of 64-grayscale voltage (negative polarity)

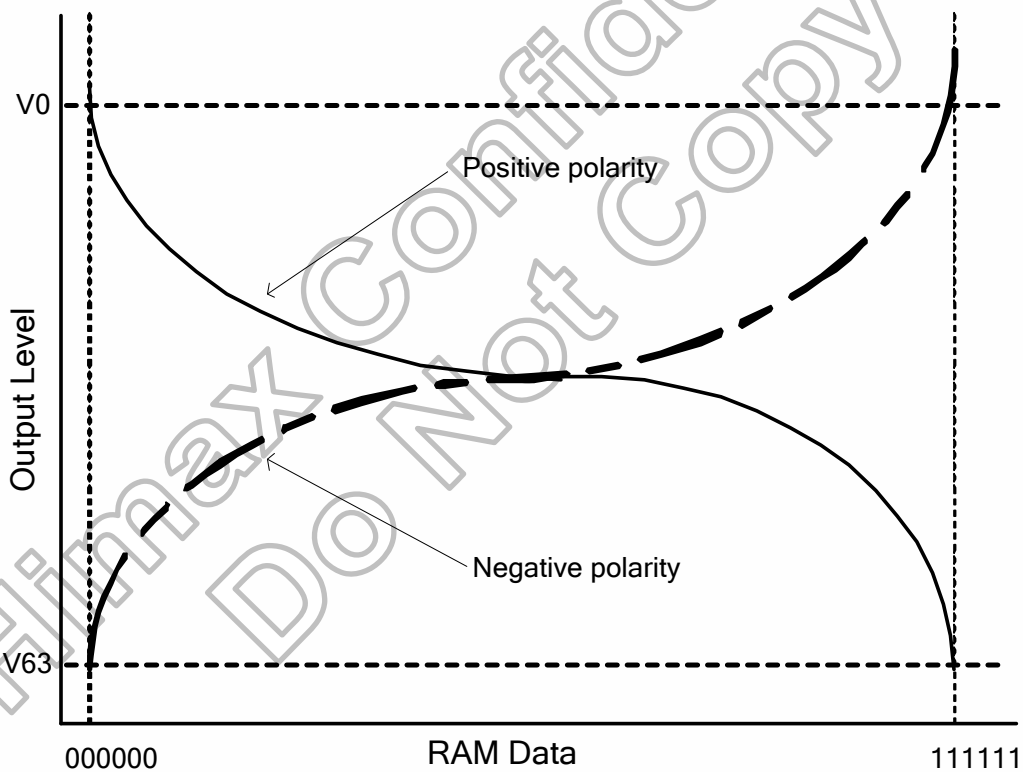
| CGMN1[1:0] | “00” | “01”  | “10”  | “11”  | CGMN0[1:0] | “00”  | “01”  | “10”  | “11”  |
|------------|------|-------|-------|-------|------------|-------|-------|-------|-------|
| CT1        | 4/5  | 34/57 | 19/47 | 3/4   | CB1        | 7/8   | 14/15 | 5/6   | 17/20 |
| CT2        | 3/5  | 4/19  | 12/47 | 21/40 | CB2        | 17/24 | 38/45 | 23/33 | 27/40 |
| CT3        | 2/5  | 7/57  | 7/47  | 13/40 | CB3        | 1/2   | 11/15 | 5/11  | 19/40 |
| CT4        | 1/5  | 1/19  | 3/47  | 3/20  | CB4        | 1/4   | 17/45 | 7/33  | 1/4   |

Table 5.31: Voltage calculation formula of grayscale voltage V59~V56 and V7~V4

**Relationship between GRAM data and output level (“Normally White Panel”, GRAM data=0)**



**Figure 5.34: Relationship between source output and Vcom**



(Same characteristic for each RGB)

**Figure 5.35: Relationship between GRAM data and output level (normal white panel REV\_Panel=“0”)**



5.10.2 Gray voltage generator for digital gamma correction nearing effect line modes

The HX8347-G digital gamma correction can reach the independent GAMMA curve of RGB. HX8347-G utilizes DGC\_LUT (Digital Gamma Correction Look Up Table) to change input data from 6-bit into 8-bit and sends 8-bit data to Dithering circuit, and then drive Source Driver via Dithering circuit. The following of the block diagram of the function.

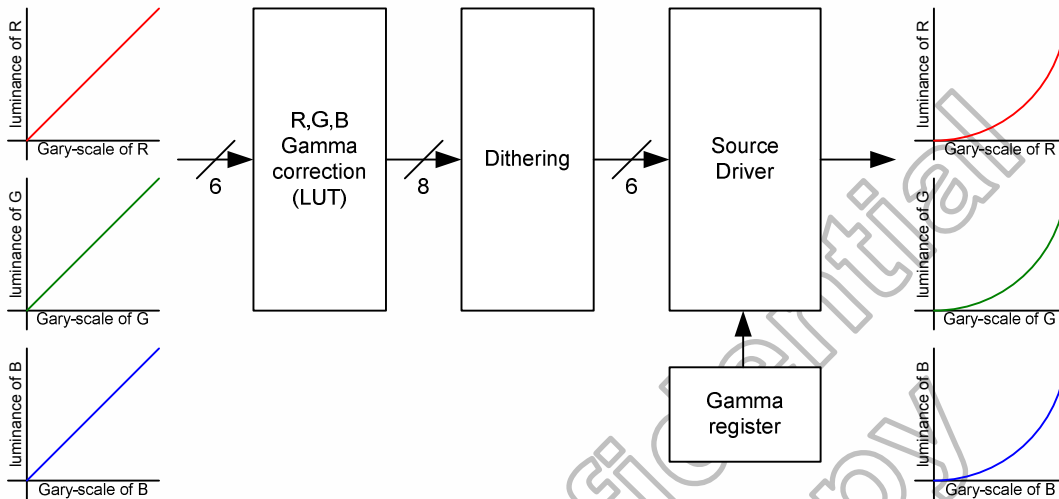


Figure 5.36: Block diagram of digital gamma correction

There are 99 bytes DGC LUT to set R, G, B gamma independently. When DGC\_EN=1, R, G, B gamma will mapping V0, V2, V4, ..., V60, V62, V63 voltage to the LUT register setting gray level voltage.  $V(2N+1) = (V(2N) + V(2N+2))/2$  (N=0~30).

| Parameter | Input (6 bit) | D7   | D6   | D5   | D4   | D3   | D2   | D1   | D0   | Default | Gray Mapping |
|-----------|---------------|------|------|------|------|------|------|------|------|---------|--------------|
| 1st       | R00h          | R007 | R006 | R005 | R004 | R003 | R002 | R001 | R000 | 00h     | R_V0         |
| 2nd       | R02h          | R017 | R016 | R015 | R014 | R013 | R012 | R011 | R010 | 08h     | R_V2         |
| 3rd       | R04h          | R027 | R026 | R025 | R024 | R023 | R022 | R021 | R020 | 10h     | R_V4         |
|           | ⋮             | ⋮    | ⋮    | ⋮    | ⋮    | ⋮    | ⋮    | ⋮    | ⋮    | ⋮       | ⋮            |
| 32nd      | R62h          | R317 | R316 | R315 | R314 | R313 | R312 | R311 | R310 | F8h     | R_V62        |
| 33rd      | R63h          | R327 | R326 | R325 | R324 | R323 | R322 | R321 | R320 | FCh     | R_V63        |
| 34th      | G00h          | G007 | G006 | G005 | G004 | G003 | G002 | G001 | G000 | 00h     | G_V0         |
| 35th      | G02h          | G017 | G016 | G015 | G014 | G013 | G012 | G011 | G010 | 08h     | G_V2         |
| 36th      | G04h          | G027 | G026 | G025 | G024 | G023 | G022 | G021 | G020 | 10h     | G_V4         |
|           | ⋮             | ⋮    | ⋮    | ⋮    | ⋮    | ⋮    | ⋮    | ⋮    | ⋮    | ⋮       | ⋮            |
| 65th      | G62h          | G317 | G316 | G315 | G314 | G313 | G312 | G311 | G310 | F8h     | G_V62        |
| 66th      | G63h          | G327 | R326 | G325 | G324 | G323 | G322 | G321 | G320 | FCh     | G_V63        |
| 67th      | B00h          | B007 | B006 | B005 | B004 | B003 | B002 | B001 | B000 | 00h     | B_V0         |
| 68th      | B02h          | B017 | B016 | B015 | B014 | B013 | B012 | B011 | B010 | 08h     | B_V2         |
| 69th      | B04h          | B027 | B026 | B025 | B024 | B023 | B022 | B021 | B020 | 10h     | B_V4         |
|           | ⋮             | ⋮    | ⋮    | ⋮    | ⋮    | ⋮    | ⋮    | ⋮    | ⋮    | ⋮       | ⋮            |
| 98th      | B62h          | B317 | B316 | B315 | B314 | B313 | B312 | B311 | B310 | F8h     | B_V62        |
| 99th      | B63h          | B327 | B326 | B325 | B324 | B323 | B322 | B321 | B320 | FCh     | B_V63        |



### 5.11 Power on/off sequence

The following are the sequences of register setting flow that applied to this driver driving the TFT display, when operate in Register-Content interface mode.

#### Display on/off set flow

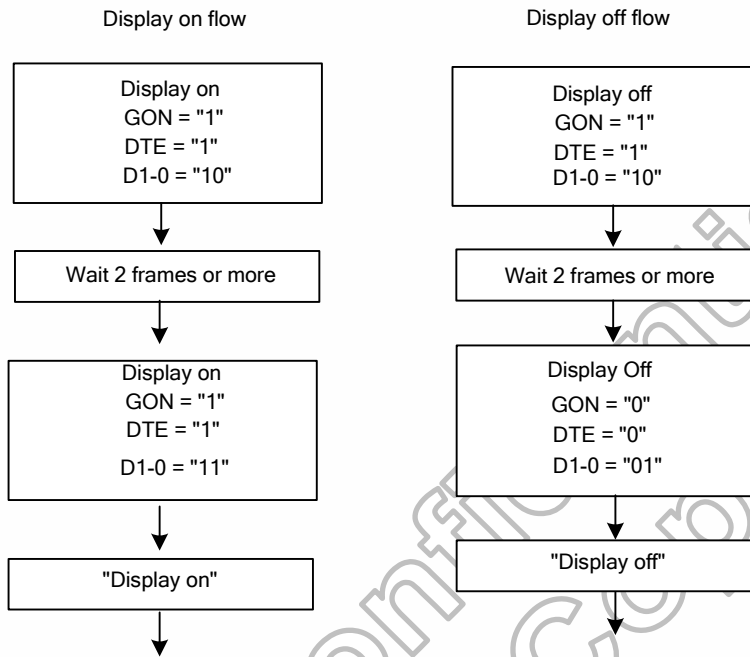
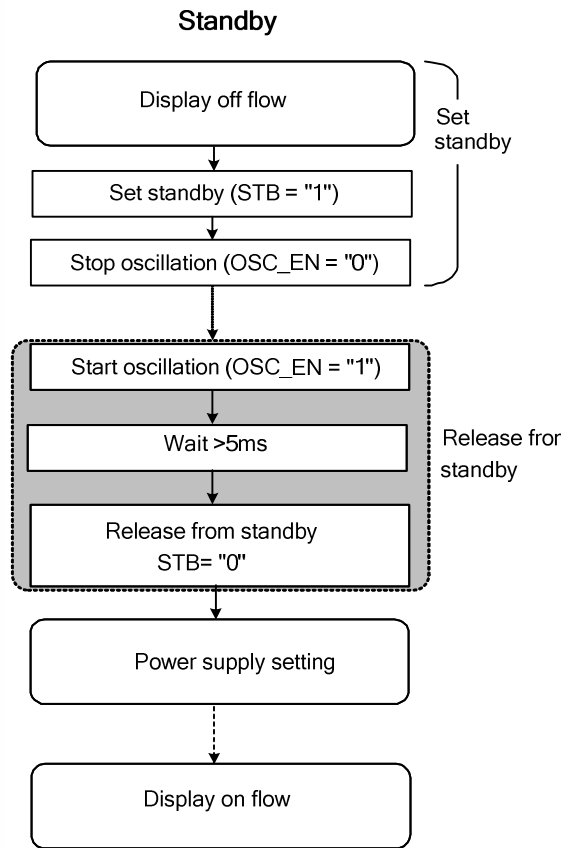


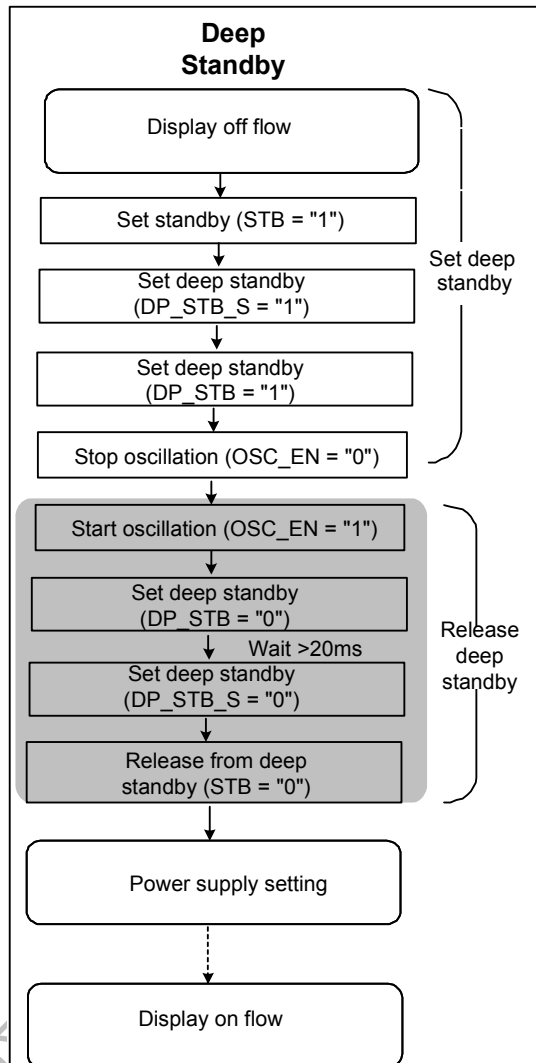
Figure 5.37: Display on/off set flow

**Standby mode set up flow**



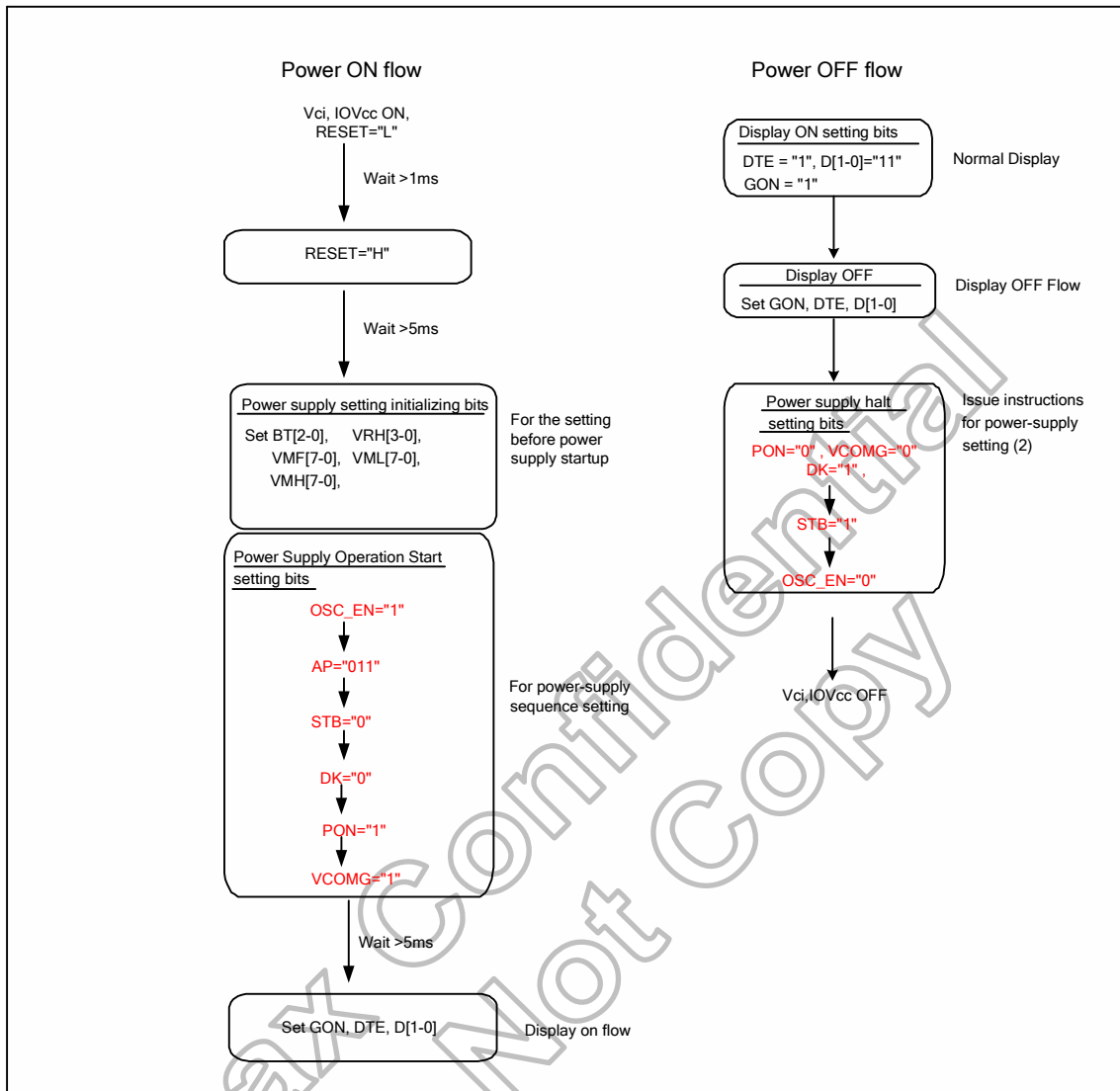
**Figure 5.38: Standby mode setting flow**

**Deep standby mode set up flow**



**Figure 5.39: Deep standby mode setting flow**

**Power on/off setting up flow**



**Figure 5.40: Power supply setting flow**

## 5.12 Input/output pin state

### 5.12.1 Output pins

| Output or Bi-directional pins  | After Power On    | After Hardware Reset |
|--------------------------------|-------------------|----------------------|
| DB17 to DB0<br>(Output driver) | High-Z (Inactive) | High-Z (Inactive)    |
| SDA                            | High-Z (Inactive) | High-Z (Inactive)    |
| TE                             | Low               | Low                  |
| BC_CTRL                        | Low               | Low                  |
| CABC_PWM_OUT                   | Low               | Low                  |

Table 5.32: Characteristics of output pins

### 5.12.2 Input pins

| Input pins                         | During Power On Process | After Power On | After Hardware Reset | During Power Off Process |
|------------------------------------|-------------------------|----------------|----------------------|--------------------------|
| NRESET                             | Input valid             | Input valid    | Input valid          | Input valid              |
| NCS                                | Input invalid           | Input valid    | Input valid          | Input invalid            |
| NWR_SCL                            | Input invalid           | Input valid    | Input valid          | Input invalid            |
| NRD                                | Input invalid           | Input valid    | Input valid          | Input invalid            |
| DNC_SCL                            | Input invalid           | Input valid    | Input valid          | Input invalid            |
| SDA                                | Input invalid           | Input valid    | Input valid          | Input invalid            |
| VSYNC                              | Input invalid           | Input valid    | Input valid          | Input invalid            |
| HSYNC                              | Input invalid           | Input valid    | Input valid          | Input invalid            |
| DE                                 | Input invalid           | Input valid    | Input valid          | Input invalid            |
| DOTCLK                             | Input invalid           | Input valid    | Input valid          | Input invalid            |
| DB[17:0]                           | Input invalid           | Input valid    | Input valid          | Input invalid            |
| OSC, IM3,IM2,<br>IM1,IM0,<br>IFSEL | Input invalid           | Input valid    | Input valid          | Input invalid            |
| TEST2-0                            | Input invalid           | Input valid    | Input valid          | Input invalid            |

Table 5.33: Characteristics of input pins

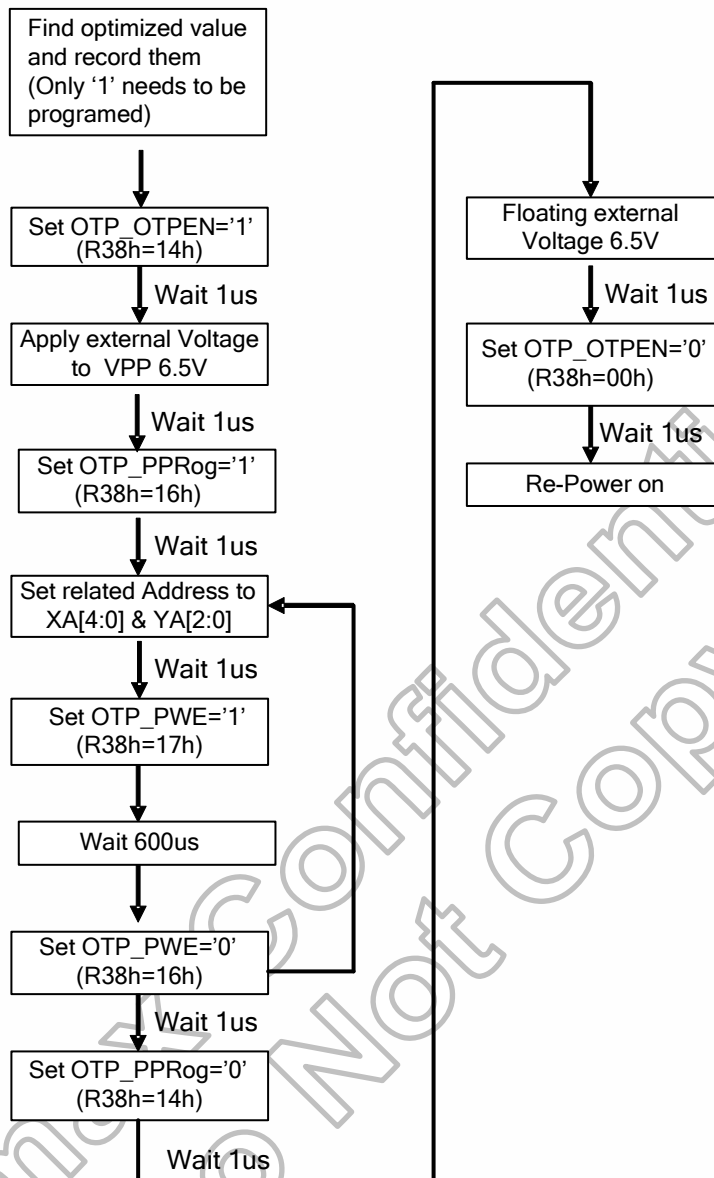
### 5.13 OTP Programing

#### 5.13.1 OTP table

|               | YA[2:0]=<br>111 | YA[2:0]=<br>110 | YA[2:0]=<br>101 | YA[2:0]=<br>100 | YA[2:0]=<br>011 | YA[2:0]=<br>010 | YA[2:0]=<br>001 | YA[2:0]=<br>000 | Non-Pro<br>gram |
|---------------|-----------------|-----------------|-----------------|-----------------|-----------------|-----------------|-----------------|-----------------|-----------------|
| XA[4:0]=00000 | ID17            | ID16            | ID15            | ID14            | ID13            | ID12            | ID11            | ID10            | 00h             |
| XA[4:0]=00001 | ID27            | ID26            | ID25            | ID24            | ID23            | ID22            | ID21            | ID20            | 00h             |
| XA[4:0]=00010 | ID37            | ID36            | ID35            | ID34            | ID33            | ID32            | ID31            | ID30            | 00h             |
| XA[4:0]=00011 | VMF17           | VMF16           | VMF15           | VMF14           | VMF13           | VMF12           | VMF11           | VMF10           | 00h             |
| XA[4:0]=00100 | VMF27           | VMF26           | VMF25           | VMF24           | VMF23           | VMF22           | VMF21           | VMF20           | 00h             |
| XA[4:0]=00101 | VMF37           | VMF36           | VMF35           | VMF34           | VMF33           | VMF32           | VMF31           | VMF30           | 00h             |
| XA[4:0]=00110 | VMH6            | VMH6            | VMH5            | VMH4            | VMH3            | VMH2            | VMH1            | VMH0            | 00h             |
| XA[4:0]=00111 | VML6            | VML6            | VML5            | VML4            | VML3            | VML2            | VML1            | VML0            | 00h             |
| XA[4:0]=01000 | Valid_ID        | -               | -               | Valid_VM<br>L   | Valid_VM<br>H   | Valid_VM<br>F3  | Valid_VM<br>F2  | Valid_VM<br>F1  | 00h             |
| XA[4:0]=01001 | Valid_pa<br>nel | -               | DDVDH_<br>TRI   | -               | SS_Pane<br>l    | GS_Pan<br>el    | REV_Pa<br>nel   | BGR_Pa<br>nel   | 00h             |

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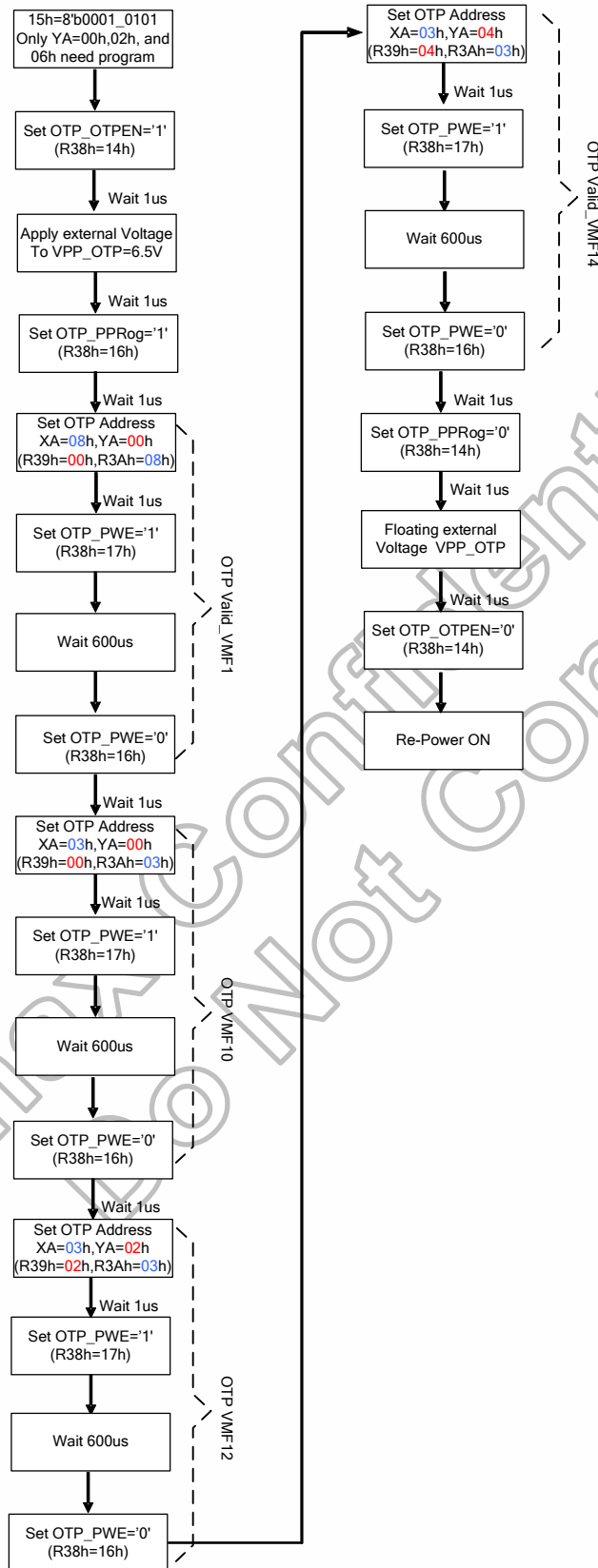
5.13.2 OTP programming flow



**Note:** Valid bit must be programmed if user wants use this OTP function.



OTP programming example (VMF=15h)

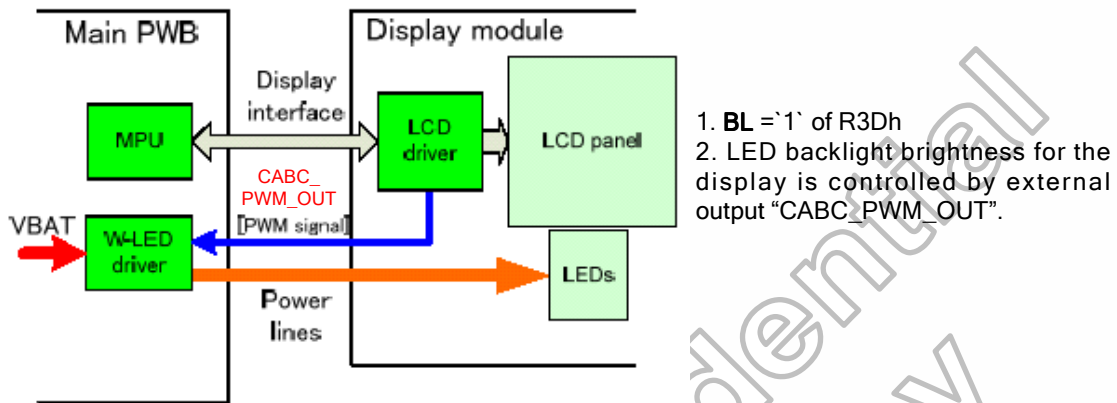




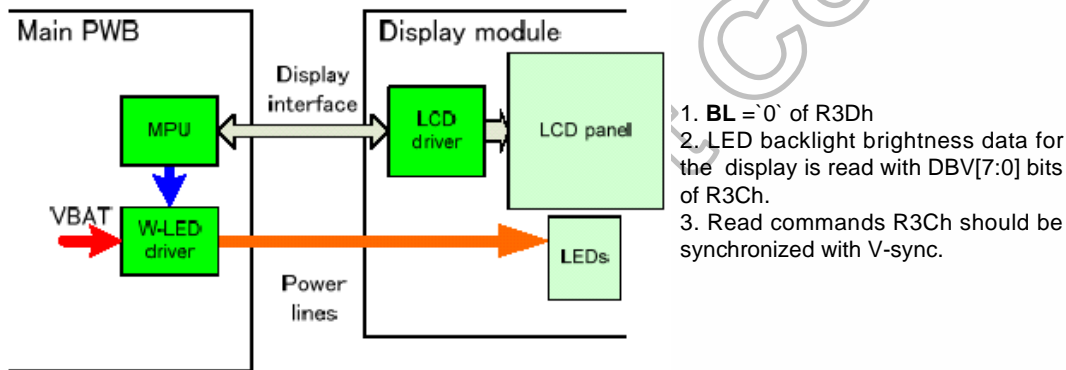
**5.14.1 Module architectures**

The HX8347-G can support two module architectures for CABC operation. The **BL** bit setting of R3Dh can be used to select used display module architecture. White LED driver circuit for display backlight is located on the main PWB, not in the display module both in architecture I and II.

• Architecture I



• Architecture II



### 5.14.2 Brightness control block

There is an external output signal from brightness block, CABC\_PWM\_OUT, to control the LED driver IC in order to control display brightness.

There are register bits, DBV[7:0] of R3Ch, for display brightness of manual brightness setting. The CABC\_PWM\_OUT duty is calculated as  $DBV[7:0]/255 \times \text{CABC duty}$  (generated after one-frame display data content analysis).

For example: CABC\_PWM\_OUT period = 2.95 ms, and DBV[7:0](R3Ch) = '228<sub>DEC</sub>' and CABC duty is 74%. Then CABC\_PWM\_OUT duty =  $228 / 255 \times 74\% \approx 65.90\%$ . Correspond to the CABC\_PWM\_OUT period = 2.95 ms, the high-level of CABC\_PWM\_OUT (high effective) = 1.94ms, and the low-level of CABC\_PWM\_OUT = 1.01ms.

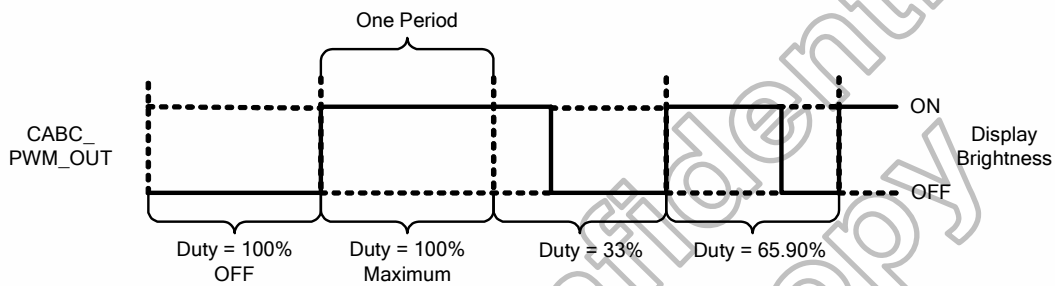


Figure 5.43: CABC\_PWM\_OUT output duty

When Architecture II module is used (**BL='0'**) with the example below, the CABC\_PWM\_OUT is always output low and the DBV[7:0](R3Ch) will be read a value as 169<sub>DEC</sub> ( $169/255 \approx 66.27\%$ ).

### 5.14.3 Minimum brightness setting of CABC function

CABC function is automatically reduced backlight brightness based on image contents. In the case of the combination with the CABC or manual brightness setting, display brightness is too dark. It must affect image quality degradation. CABC minimum brightness setting (**CMB[7:0]** bits of R3Fh) works to avoid too much brightness reduction.

When CABC is active, CABC can not reduce the display brightness to less than CABC minimum brightness setting. Image processing function works as normal, even if the brightness can not be changed.

This function does not affect the other function, manual brightness setting. Manual brightness can be set the display brightness to less than CABC minimum brightness. Smooth transition and dimming function can work as normal.

When display brightness is turned off (**BCTRL='0'** of R3Dh), CABC minimum brightness setting is ignored. Read CABC minimum brightness **CMB[7:0]** (R3Fh) always reads the setting value.

### 5.14.4 Display dimming

A dimming function (how fast to change the brightness from old to new level and what are brightness levels during the change) is used when changing from one brightness level to another to avoid flicker in the actual display module. This dimming function curve is the same in increment and decrement directions.

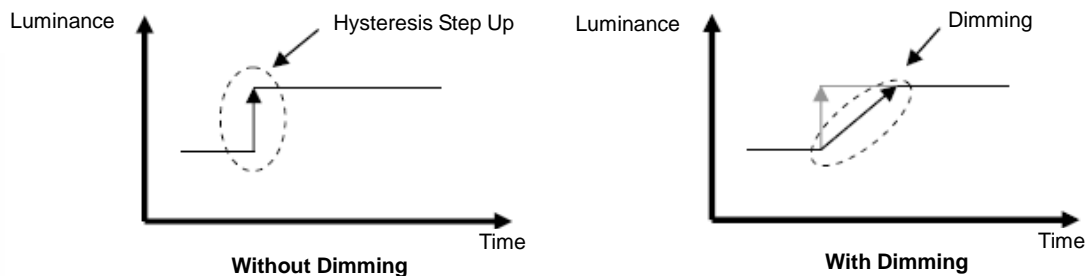


Figure 5.44: Dimming function

## 6. Command



## 6.1 Command set

| (Hex) | Operation Code                   | W/R | Upper Code | Lower Code                |             |              |        |                         |                    |             |           | Comment |
|-------|----------------------------------|-----|------------|---------------------------|-------------|--------------|--------|-------------------------|--------------------|-------------|-----------|---------|
|       |                                  |     | D[17:8]    | D7                        | D6          | D5           | D4     | D3                      | D2                 | D1          | D0        |         |
| 00    | Himax ID                         | R   | -          | 0                         | 1           | 1            | 1      | 0                       | 1                  | 0           | 1         | -       |
| 01    | Display Mode control             | W/R | -          | DP_S TB(0)                | DP_STB_S(0) | -            | -      | SCROL (0)               | IDMON (0)          | INNON (0)   | PTLON (0) | -       |
| 02    | Column address start 2           | W/R | -          | SC[15:8] (8'b0000_0000)   |             |              |        |                         |                    |             |           | -       |
| 03    | Column address start 1           | W/R | -          | SC[7:0] (8'b0000_0000)    |             |              |        |                         |                    |             |           | -       |
| 04    | Column address end 2             | W/R | -          | EC[15:8] (8'b0000_0000)   |             |              |        |                         |                    |             |           | -       |
| 05    | Column address end 1             | W/R | -          | EC[7:0] (8'b1110_1111)    |             |              |        |                         |                    |             |           | -       |
| 06    | Row address start 2              | W/R | -          | SP[15:8] (8'b0000_0000)   |             |              |        |                         |                    |             |           | -       |
| 07    | Row address start 1              | W/R | -          | SP[7:0] (8'b0000_0000)    |             |              |        |                         |                    |             |           | -       |
| 08    | Row address end 2                | W/R | -          | EP[15:8] (8'b0000_0001)   |             |              |        |                         |                    |             |           | -       |
| 09    | Row address end 1                | W/R | -          | EP[7:0] (8'b0011_1111)    |             |              |        |                         |                    |             |           | -       |
| 0A    | Partial area start row 2         | W/R | -          | PSL[15:8] (8'b0000_0000)  |             |              |        |                         |                    |             |           | -       |
| 0B    | Partial area start row 1         | W/R | -          | PSL[7:0] (8'b0000_0000)   |             |              |        |                         |                    |             |           | -       |
| 0C    | Partial area end row 2           | W/R | -          | PEL[15:8] (8'b0000_0001)  |             |              |        |                         |                    |             |           | -       |
| 0D    | Partial area end row 1           | W/R | -          | PEL[7:0] (8'b0011_1111)   |             |              |        |                         |                    |             |           | -       |
| 0E    | Vertical Scroll Top fixed area 2 | W/R | -          | TFA[15:8] (8'b0000_0000)  |             |              |        |                         |                    |             |           | -       |
| 0F    | Vertical Scroll Top fixed area 1 | W/R | -          | TFA[7:0] (8'b0000_0000)   |             |              |        |                         |                    |             |           | -       |
| 10    | Vertical Scroll height area 2    | W/R | -          | VSA[15:8] (8'b0000_0001)  |             |              |        |                         |                    |             |           | -       |
| 11    | Vertical Scroll height area 1    | W/R | -          | VSA[7:0] (8'b0100_0000)   |             |              |        |                         |                    |             |           | -       |
| 12    | Vertical Scroll Button area 2    | W/R | -          | BFA[15:8] (8'b0000_0000)  |             |              |        |                         |                    |             |           | -       |
| 13    | Vertical Scroll Button area 1    | W/R | -          | BFA [7:0] (8'b0000_0000)  |             |              |        |                         |                    |             |           | -       |
| 14    | Vertical Scroll Start address 2  | W/R | -          | VSP [15:8] (8'b0000_0000) |             |              |        |                         |                    |             |           | -       |
| 15    | Vertical Scroll Start address 1  | W/R | -          | VSP [7:0] (8'b0000_0000)  |             |              |        |                         |                    |             |           | -       |
| 16    | Memory Access control            | W/R | -          | MY(0)                     | MX(0)       | MV(0)        | ML(0)  | BGR(0)                  | -                  | -           | -         | -       |
| 17    | COLMOD                           | W/R | -          | CSEL[3:0] (4b'0110)       |             |              |        | -                       | IFPF[2:0] (3b'110) |             |           | -       |
| 18    | OSC Control 2                    | W/R | -          | I/PI_RADJ1[3:0] (3b'0011) |             |              |        | N/P_RADJ0[3:0](4b'0100) |                    |             |           | -       |
| 19    | OSC Control 1                    | W/R | -          | -                         | -           | -            | -      | -                       | -                  | -           | OSC_EN(0) | -       |
| 1A    | Power Control 1                  | W/R | -          | -                         | -           | -            | -      | BT[2:0] (001)           |                    |             |           | -       |
| 1B    | Power Control 2                  | W/R | -          | VRH[5:0] (01_1011)_4.8V   |             |              |        |                         |                    |             |           | -       |
| 1C    | Power Control 3                  | W/R | -          | -                         | -           | -            | -      | AP[2:0] (011)           |                    |             | -         |         |
| 1D    | Power Control 4                  | W/R | -          | I/PI_FS0[2:0](100)        |             |              |        | -                       | N/P_FS0[2:0] (100) |             |           | -       |
| 1E    | Power Control 5                  | W/R | -          | I/PI_FS1[2:0] (100)       |             |              |        | -                       | N/P_FS1[2:0] (100) |             |           | -       |
| 1F    | Power Control 6                  | W/R | -          | GASEN(1)                  | VCOMG(0)    | -            | PON(0) | DK(1)                   | XDK(0)             | DDVDH_TR(0) | STB(1)    | -       |
| 22    | SRAM Write Control               | W/R | SRAM Write |                           |             |              |        |                         |                    |             |           | -       |
| 23    | VCOM Control 1                   | W/R | -          | VMF[7:0](1000_0000)       |             |              |        |                         |                    |             |           | -       |
| 24    | VCOM Control 2                   | W/R | -          | VMH[7:0](0010_1111)       |             |              |        |                         |                    |             |           | -       |
| 25    | VCOM Control 3                   | W/R | -          | VML[7:0](0101_0111)       |             |              |        |                         |                    |             |           | -       |
| 26    | Display Control 1                | W/R | -          | --                        | -           | -            | -      | ISC[3:0](0001)          |                    |             | -         |         |
| 27    | Display Control 2                | W/R | -          | PT[1:0](10)               |             | PTV[1:0](10) |        | -                       | -                  | PTG(1)      | REF(1)    | -       |



| (Hex) | Operation Code          | W/R | Upper Code | Lower Code                   |                      |                   |                |                    |                      |                  |               | Comment |
|-------|-------------------------|-----|------------|------------------------------|----------------------|-------------------|----------------|--------------------|----------------------|------------------|---------------|---------|
|       |                         |     | D[17:8]    | D7                           | D6                   | D5                | D4             | D3                 | D2                   | D1               | D0            |         |
| 28    | Display Control 3       | W/R | -          | -                            | -                    | GON(1)            | DTE(0)         | D[1:0] (00)        |                      | -                | -             | -       |
| 29    | Frame Rate control 1    | W/R | -          | I/PI_RTN[3:0](1000)          |                      |                   |                | N/P_RTN[3:0](1000) |                      |                  |               | -       |
| 2A    | Frame Rate Control 2    | W/R | -          | -                            | -                    | I/PI_DIV[1:0](00) |                | -                  | -                    | N/P_DIV[1:0](00) |               | -       |
| 2B    | Frame Rate Control 3    | W/R | -          | N/P_DUM[7:0] (8b'0001_1100)  |                      |                   |                |                    |                      |                  |               | -       |
| 2C    | Frame Rate Control 4    | W/R | -          | I/PI_DUM[7:0] (8b'0001_1100) |                      |                   |                |                    |                      |                  |               | -       |
| 2D    | Cycle Control 1         | W/R | -          | GDON[7:0] (8'b0000_1101)     |                      |                   |                |                    |                      |                  |               | -       |
| 2E    | Cycle Control 2         | W/R | -          | GDOF[7:0] (8'b0111_1000)     |                      |                   |                |                    |                      |                  |               | -       |
| 2F    | Display inversion       | W/R | -          | -                            | I/PI_NW[2:0](3b'001) |                   |                | -                  | N/P_NW[2:0] (3b'001) |                  |               | -       |
| 31    | RGB interface control 1 | W/R | -          | -                            | -                    | -                 | -              | -                  | -                    | RCM[1:0](00)     |               | -       |
| 32    | RGB interface control 2 | W/R | -          | -                            | -                    | -                 | -              | DPL (0)            | HSPL (0)             | VSPL (0)         | EPL (0)       | -       |
| 33    | RGB interface control 3 | W/R | -          | HBP[7:0]                     |                      |                   |                |                    |                      |                  |               | -       |
| 34    | RGB interface control 4 | W/R | -          | HBP[9:8]                     |                      |                   | VBP[5:0]       |                    |                      |                  |               | -       |
| 36    | Panel Characteristic    | W/R | -          | -                            | -                    | -                 | -              | SS_P<br>anel       | GS_Pan<br>el         | REV_P<br>anel    | BGR_P<br>anel | -       |
| 38    | OTP Control 1           | W/R | -          | OTP_PTM[1:0]                 |                      | OTP_VARDJ[1:0]    |                | OTP_POR            | OTP_OTPEN            | OTP_P<br>PROG    | OTP_P<br>WE   | -       |
| 39    | OTP Control 2           | W/R | -          | -                            | -                    | -                 | -              | -                  | OTP_YA<br>2          | OTP_YA1          | OTP_Y<br>A0   | -       |
| 3A    | OTP Control 3           | W/R | -          | -                            | -                    | -                 | OTP_XA<br>4    | OTP_XA3            | OTP_XA<br>2          | OTP_XA1          | OTP_XA0       | -       |
| 3B    | OTP Control 4           | R   | -          | OTPD<br>TA7                  | OTPD<br>ATA6         | OTPD<br>TA5       | OTPDAT<br>A4   | OTPD<br>ATA3       | OTPDAT<br>A2         | OTPDAT<br>A1     | OTPDAT<br>0   | -       |
| 3C    | CABC Control 1          | W/R | -          | DBV[7:0](8'h00)              |                      |                   |                |                    |                      |                  |               | -       |
| 3D    | CABC Control 2          | W/R | -          | -                            | -                    | BCTRL<br>(0)      | -              | DD<br>(0)          | BL<br>(0)            | -                | -             | -       |
| 3E    | CABC Control 3          | W/R | -          | -                            | -                    | -                 | -              | -                  | -                    | C1<br>(0)        | C0<br>(0)     | -       |
| 3F    | CABC Control 4          | W/R | -          | CMB[7:0](8'h00)              |                      |                   |                |                    |                      |                  |               | -       |
| 40    | r1 Control (1)          | W/R | -          | -                            | -                    | -                 | -              | VRP0[5:0]          |                      |                  |               | -       |
| 41    | r1 Control (2)          | W/R | -          | -                            | -                    | -                 | -              | VRP1[5:0]          |                      |                  |               | -       |
| 42    | r1 Control (3)          | W/R | -          | -                            | -                    | -                 | -              | VRP2[5:0]          |                      |                  |               | -       |
| 43    | r1 Control (4)          | W/R | -          | -                            | -                    | -                 | -              | VRP3[5:0]          |                      |                  |               | -       |
| 44    | r1 Control (5)          | W/R | -          | -                            | -                    | -                 | -              | VRP4[5:0]          |                      |                  |               | -       |
| 45    | r1 Control (6)          | W/R | -          | -                            | -                    | -                 | -              | VRP5[5:0]          |                      |                  |               | -       |
| 46    | r1 Control (7)          | W/R | -          | -                            | -                    | -                 | -              | PRP0[6:0]          |                      |                  |               | -       |
| 47    | r1 Control (8)          | W/R | -          | -                            | -                    | -                 | -              | PRP1[6:0]          |                      |                  |               | -       |
| 48    | r1 Control (9)          | W/R | -          | -                            | -                    | -                 | -              | PKP0[4:0]          |                      |                  |               | -       |
| 49    | r1 Control (10)         | W/R | -          | -                            | -                    | -                 | -              | PKP1[4:0]          |                      |                  |               | -       |
| 4A    | r1 Control (11)         | W/R | -          | -                            | -                    | -                 | -              | PKP2[4:0]          |                      |                  |               | -       |
| 4B    | r1 Control (12)         | W/R | -          | -                            | -                    | -                 | -              | PKP3[4:0]          |                      |                  |               | -       |
| 4C    | r1 Control (13)         | W/R | -          | -                            | -                    | -                 | -              | PKP4[4:0]          |                      |                  |               | -       |
| 50    | r1 Control (14)         | W/R | -          | -                            | -                    | -                 | -              | VRN0[5:0]          |                      |                  |               | -       |
| 51    | r1 Control (15)         | W/R | -          | -                            | -                    | -                 | -              | VRN1[5:0]          |                      |                  |               | -       |
| 52    | r1 Control (16)         | W/R | -          | -                            | -                    | -                 | -              | VRN2[5:0]          |                      |                  |               | -       |
| 53    | r1 Control (17)         | W/R | -          | -                            | -                    | -                 | -              | VRN3[5:0]          |                      |                  |               | -       |
| 54    | r1 Control (18)         | W/R | -          | -                            | -                    | -                 | -              | VRN4[5:0]          |                      |                  |               | -       |
| 55    | r1 Control (19)         | W/R | -          | -                            | -                    | -                 | -              | VRN5[5:0]          |                      |                  |               | -       |
| 56    | r1 Control (20)         | W/R | -          | -                            | -                    | -                 | -              | PRN0[6:0]          |                      |                  |               | -       |
| 57    | r1 Control (21)         | W/R | -          | -                            | -                    | -                 | -              | PRN1[6:0]          |                      |                  |               | -       |
| 58    | r1 Control (22)         | W/R | -          | -                            | -                    | -                 | -              | PKN0[4:0]          |                      |                  |               | -       |
| 59    | r1 Control (23)         | W/R | -          | -                            | -                    | -                 | -              | PKN1[4:0]          |                      |                  |               | -       |
| 5A    | r1 Control (24)         | W/R | -          | -                            | -                    | -                 | -              | PKN2[4:0]          |                      |                  |               | -       |
| 5B    | r1 Control (25)         | W/R | -          | -                            | -                    | -                 | -              | PKN3[4:0]          |                      |                  |               | -       |
| 5C    | r1 Control (26)         | W/R | -          | -                            | -                    | -                 | -              | PKN4[4:0]          |                      |                  |               | -       |
| 5D    | r1 Control (27)         | W/R | -          | CGMN1[1:0]                   |                      | CGMN0[1:0]        |                | CGMP1[1:0]         |                      | CGMP0[1:0]       |               | -       |
| 60    | TE Control              | W/R | -          | -                            | -                    | -                 | TE_mod<br>e(0) | TEOE(0)            | -                    | -                | -             | -       |
| 61    | ID1                     | W/R | -          | ID17                         | ID16                 | ID15              | ID14           | ID13               | ID12                 | ID11             | ID10          | -       |
| 62    | ID2                     | W/R | -          | ID27                         | ID26                 | ID25              | ID24           | ID23               | ID22                 | ID21             | ID20          | -       |
| 63    | ID3                     | W/R | -          | ID37                         | ID36                 | ID35              | ID34           | ID33               | ID32                 | ID31             | ID30          | -       |

| (Hex) | Operation Code                  | W/R | Upper Code | Lower Code  |         |          |          |         |         |        |                    | Comment |
|-------|---------------------------------|-----|------------|-------------|---------|----------|----------|---------|---------|--------|--------------------|---------|
|       |                                 |     | D[17:8]    | D7          | D6      | D5       | D4       | D3      | D2      | D1     | D0                 |         |
| 84    | TE Output line2                 | W/R | -          | TESEL15     | TESEL14 | TESEL 13 | TESEL 12 | TESEL11 | TESEL10 | TESEL9 | TESEL8             | -       |
| 85    | TE Output line1                 | W/R | -          | TESEL 7     | TESEL 6 | TESEL 5  | TESEL 4  | TESEL 3 | TESEL 2 | TESEL1 | TESEL 0            | -       |
| E4    | Power saving 1                  | W/R | -          | EQ_S1[7:0]  |         |          |          |         |         |        |                    | -       |
| E5    | Power saving 2                  | W/R | -          | EQ_S2[7:0]  |         |          |          |         |         |        |                    | -       |
| E6    | Power saving 3                  | W/R | -          | EQ_S3[7:0]  |         |          |          |         |         |        |                    | -       |
| E7    | Power saving 4                  | W/R | -          | EQ_S4[7:0]  |         |          |          |         |         |        |                    | -       |
| E8    | Source OP control_Normal        | W/R | -          | OPON_N[7:0] |         |          |          |         |         |        |                    | -       |
| E9    | Source OP control_IDLE          | W/R | -          | OPON_I[7:0] |         |          |          |         |         |        |                    | -       |
| EA    | Power control internal use (1)  | W/R | -          | STBA[15:8]  |         |          |          |         |         |        |                    | -       |
| EB    | Power control internal use (2)  | W/R | -          | STBA[7:0]   |         |          |          |         |         |        |                    | -       |
| EC    | Source control internal use (1) | W/R | -          | PTBA[15:8]  |         |          |          |         |         |        |                    | -       |
| ED    | Source control internal use (2) | W/R | -          | PTBA[7:0]   |         |          |          |         |         |        |                    | -       |
| FF    | Page select                     | W/R | -          | -           | -       | -        | -        | -       | -       | -      | PAGE_SEL[1:0] (00) | -       |

Table 6.1: List table of command set page 0

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| (Hex) | Operation Code | W/R | Upper Code | Lower Code         |    |    |    |    |    |    |    | Comment   |   |
|-------|----------------|-----|------------|--------------------|----|----|----|----|----|----|----|-----------|---|
|       |                |     | D[17:8]    | D7                 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |           |   |
| R00h  | DGC Control    | W/R | -          | -                  | -  | -  | -  | -  | -  | -  | -  | DGC_EN(0) | - |
| R01h  | DGC LUT1       | W/R | -          | DGC_LUT_R00(8'h00) |    |    |    |    |    |    |    | -         |   |
| R02h  | DGC LUT2       | W/R | -          | DGC_LUT_R01(8'h08) |    |    |    |    |    |    |    | -         |   |
| R03h  | DGC LUT3       | W/R | -          | DGC_LUT_R02(8'h10) |    |    |    |    |    |    |    | -         |   |
| R04h  | DGC LUT4       | W/R | -          | DGC_LUT_R03(8'h18) |    |    |    |    |    |    |    | -         |   |
| R05h  | DGC LUT5       | W/R | -          | DGC_LUT_R04(8'h20) |    |    |    |    |    |    |    | -         |   |
| R06h  | DGC LUT6       | W/R | -          | DGC_LUT_R05(8'h28) |    |    |    |    |    |    |    | -         |   |
| R07h  | DGC LUT7       | W/R | -          | DGC_LUT_R06(8'h30) |    |    |    |    |    |    |    | -         |   |
| R08h  | DGC LUT8       | W/R | -          | DGC_LUT_R07(8'h38) |    |    |    |    |    |    |    | -         |   |
| R09h  | DGC LUT9       | W/R | -          | DGC_LUT_R08(8'h40) |    |    |    |    |    |    |    | -         |   |
| R0Ah  | DGC LUT10      | W/R | -          | DGC_LUT_R09(8'h48) |    |    |    |    |    |    |    | -         |   |
| R0Bh  | DGC LUT11      | W/R | -          | DGC_LUT_R10(8'h50) |    |    |    |    |    |    |    | -         |   |
| R0Ch  | DGC LUT12      | W/R | -          | DGC_LUT_R11(8'h58) |    |    |    |    |    |    |    | -         |   |
| R0Dh  | DGC LUT13      | W/R | -          | DGC_LUT_R12(8'h60) |    |    |    |    |    |    |    | -         |   |
| R0Eh  | DGC LUT14      | W/R | -          | DGC_LUT_R13(8'h68) |    |    |    |    |    |    |    | -         |   |
| R0Fh  | DGC LUT15      | W/R | -          | DGC_LUT_R14(8'h70) |    |    |    |    |    |    |    | -         |   |
| R10h  | DGC LUT16      | W/R | -          | DGC_LUT_R15(8'h78) |    |    |    |    |    |    |    | -         |   |
| R11h  | DGC LUT17      | W/R | -          | DGC_LUT_R16(8'h80) |    |    |    |    |    |    |    | -         |   |
| R12h  | DGC LUT18      | W/R | -          | DGC_LUT_R17(8'h88) |    |    |    |    |    |    |    | -         |   |
| R13h  | DGC LUT19      | W/R | -          | DGC_LUT_R18(8'h90) |    |    |    |    |    |    |    | -         |   |
| R14h  | DGC LUT20      | W/R | -          | DGC_LUT_R19(8'h98) |    |    |    |    |    |    |    | -         |   |
| R15h  | DGC LUT21      | W/R | -          | DGC_LUT_R20(8'hA0) |    |    |    |    |    |    |    | -         |   |
| R16h  | DGC LUT22      | W/R | -          | DGC_LUT_R21(8'hA8) |    |    |    |    |    |    |    | -         |   |
| R17h  | DGC LUT23      | W/R | -          | DGC_LUT_R22(8'hB0) |    |    |    |    |    |    |    | -         |   |
| R18h  | DGC LUT24      | W/R | -          | DGC_LUT_R23(8'hB8) |    |    |    |    |    |    |    | -         |   |
| R19h  | DGC LUT25      | W/R | -          | DGC_LUT_R24(8'hC0) |    |    |    |    |    |    |    | -         |   |
| R1Ah  | DGC LUT26      | W/R | -          | DGC_LUT_R25(8'hC8) |    |    |    |    |    |    |    | -         |   |
| R1Bh  | DGC LUT27      | W/R | -          | DGC_LUT_R26(8'hD0) |    |    |    |    |    |    |    | -         |   |
| R1Ch  | DGC LUT28      | W/R | -          | DGC_LUT_R27(8'hD8) |    |    |    |    |    |    |    | -         |   |
| R1Dh  | DGC LUT29      | W/R | -          | DGC_LUT_R28(8'hE0) |    |    |    |    |    |    |    | -         |   |
| R1Eh  | DGC LUT30      | W/R | -          | DGC_LUT_R29(8'hE8) |    |    |    |    |    |    |    | -         |   |
| R1Fh  | DGC LUT31      | W/R | -          | DGC_LUT_R30(8'hF0) |    |    |    |    |    |    |    | -         |   |
| R20h  | DGC LUT32      | W/R | -          | DGC_LUT_R31(8'hF8) |    |    |    |    |    |    |    | -         |   |
| R21h  | DGC LUT33      | W/R | -          | DGC_LUT_R32(8'hFC) |    |    |    |    |    |    |    | -         |   |
| R22h  | DGC LUT34      | W/R | -          | DGC_LUT_G00(8'h00) |    |    |    |    |    |    |    | -         |   |
| R23h  | DGC LUT35      | W/R | -          | DGC_LUT_G01(8'h08) |    |    |    |    |    |    |    | -         |   |
| R24h  | DGC LUT36      | W/R | -          | DGC_LUT_G02(8'h10) |    |    |    |    |    |    |    | -         |   |
| R25h  | DGC LUT37      | W/R | -          | DGC_LUT_G03(8'h18) |    |    |    |    |    |    |    | -         |   |
| R26h  | DGC LUT38      | W/R | -          | DGC_LUT_G04(8'h20) |    |    |    |    |    |    |    | -         |   |
| R27h  | DGC LUT39      | W/R | -          | DGC_LUT_G05(8'h28) |    |    |    |    |    |    |    | -         |   |
| R28h  | DGC LUT40      | W/R | -          | DGC_LUT_G06(8'h30) |    |    |    |    |    |    |    | -         |   |
| R29h  | DGC LUT41      | W/R | -          | DGC_LUT_G07(8'h38) |    |    |    |    |    |    |    | -         |   |
| R2Ah  | DGC LUT42      | W/R | -          | DGC_LUT_G08(8'h40) |    |    |    |    |    |    |    | -         |   |
| R2Bh  | DGC LUT43      | W/R | -          | DGC_LUT_G09(8'h48) |    |    |    |    |    |    |    | -         |   |
| R2Ch  | DGC LUT44      | W/R | -          | DGC_LUT_G10(8'h50) |    |    |    |    |    |    |    | -         |   |
| R2Dh  | DGC LUT45      | W/R | -          | DGC_LUT_G11(8'h58) |    |    |    |    |    |    |    | -         |   |
| R2Eh  | DGC LUT46      | W/R | -          | DGC_LUT_G12(8'h60) |    |    |    |    |    |    |    | -         |   |
| R2Fh  | DGC LUT47      | W/R | -          | DGC_LUT_G13(8'h68) |    |    |    |    |    |    |    | -         |   |
| R30h  | DGC LUT48      | W/R | -          | DGC_LUT_G14(8'h70) |    |    |    |    |    |    |    | -         |   |
| R31h  | DGC LUT49      | W/R | -          | DGC_LUT_G15(8'h78) |    |    |    |    |    |    |    | -         |   |
| R32h  | DGC LUT50      | W/R | -          | DGC_LUT_G16(8'h80) |    |    |    |    |    |    |    | -         |   |
| R33h  | DGC LUT51      | W/R | -          | DGC_LUT_G17(8'h88) |    |    |    |    |    |    |    | -         |   |
| R34h  | DGC LUT52      | W/R | -          | DGC_LUT_G18(8'h90) |    |    |    |    |    |    |    | -         |   |
| R35h  | DGC LUT53      | W/R | -          | DGC_LUT_G19(8'h98) |    |    |    |    |    |    |    | -         |   |
| R36h  | DGC LUT54      | W/R | -          | DGC_LUT_G20(8'hA0) |    |    |    |    |    |    |    | -         |   |
| R37h  | DGC LUT55      | W/R | -          | DGC_LUT_G21(8'hA8) |    |    |    |    |    |    |    | -         |   |
| R38h  | DGC LUT56      | W/R | -          | DGC_LUT_G22(8'hB0) |    |    |    |    |    |    |    | -         |   |
| R39h  | DGC LUT57      | W/R | -          | DGC_LUT_G23(8'hB8) |    |    |    |    |    |    |    | -         |   |
| R3Ah  | DGC LUT58      | W/R | -          | DGC_LUT_G24(8'hC0) |    |    |    |    |    |    |    | -         |   |
| R3Bh  | DGC LUT59      | W/R | -          | DGC_LUT_G25(8'hC8) |    |    |    |    |    |    |    | -         |   |
| R3Ch  | DGC LUT60      | W/R | -          | DGC_LUT_G26(8'hD0) |    |    |    |    |    |    |    | -         |   |
| R3Dh  | DGC LUT61      | W/R | -          | DGC_LUT_G27(8'hD8) |    |    |    |    |    |    |    | -         |   |
| R3Eh  | DGC LUT62      | W/R | -          | DGC_LUT_G28(8'hE0) |    |    |    |    |    |    |    | -         |   |
| R3Fh  | DGC LUT63      | W/R | -          | DGC_LUT_G29(8'hE8) |    |    |    |    |    |    |    | -         |   |
| R40h  | DGC LUT64      | W/R | -          | DGC_LUT_G30(8'hF0) |    |    |    |    |    |    |    | -         |   |
| R41h  | DGC LUT65      | W/R | -          | DGC_LUT_G31(8'hF8) |    |    |    |    |    |    |    | -         |   |
| R42h  | DGC LUT66      | W/R | -          | DGC_LUT_G32(8'hFC) |    |    |    |    |    |    |    | -         |   |

| (Hex) | Operation Code         | W/R | Upper Code | Lower Code            |                  |    |    |    |    |                    |    | Comment |
|-------|------------------------|-----|------------|-----------------------|------------------|----|----|----|----|--------------------|----|---------|
|       |                        |     | D[17:8]    | D7                    | D6               | D5 | D4 | D3 | D2 | D1                 | D0 |         |
| R43h  | DGC LUT67              | W/R | -          | DGC_LUT_B00(8'h00)    |                  |    |    |    |    |                    |    | -       |
| R44h  | DGC LUT68              | W/R | -          | DGC_LUT_B01(8'h08)    |                  |    |    |    |    |                    |    | -       |
| R45h  | DGC LUT69              | W/R | -          | DGC_LUT_B02(8'h10)    |                  |    |    |    |    |                    |    | -       |
| R46h  | DGC LUT70              | W/R | -          | DGC_LUT_B03(8'h18)    |                  |    |    |    |    |                    |    | -       |
| R47h  | DGC LUT71              | W/R | -          | DGC_LUT_B04(8'h20)    |                  |    |    |    |    |                    |    | -       |
| R48h  | DGC LUT72              | W/R | -          | DGC_LUT_B05(8'h28)    |                  |    |    |    |    |                    |    | -       |
| R49h  | DGC LUT73              | W/R | -          | DGC_LUT_B06(8'h30)    |                  |    |    |    |    |                    |    | -       |
| R4Ah  | DGC LUT74              | W/R | -          | DGC_LUT_B07(8'h38)    |                  |    |    |    |    |                    |    | -       |
| R4Bh  | DGC LUT75              | W/R | -          | DGC_LUT_B08(8'h40)    |                  |    |    |    |    |                    |    | -       |
| R4Ch  | DGC LUT76              | W/R | -          | DGC_LUT_B09(8'h48)    |                  |    |    |    |    |                    |    | -       |
| R4Dh  | DGC LUT77              | W/R | -          | DGC_LUT_B10(8'h50)    |                  |    |    |    |    |                    |    | -       |
| R4Eh  | DGC LUT78              | W/R | -          | DGC_LUT_B11(8'h58)    |                  |    |    |    |    |                    |    | -       |
| R4Fh  | DGC LUT79              | W/R | -          | DGC_LUT_B12(8'h60)    |                  |    |    |    |    |                    |    | -       |
| R50h  | DGC LUT80              | W/R | -          | DGC_LUT_B13(8'h68)    |                  |    |    |    |    |                    |    | -       |
| R51h  | DGC LUT81              | W/R | -          | DGC_LUT_B14(8'h70)    |                  |    |    |    |    |                    |    | -       |
| R52h  | DGC LUT82              | W/R | -          | DGC_LUT_B15(8'h78)    |                  |    |    |    |    |                    |    | -       |
| R53h  | DGC LUT83              | W/R | -          | DGC_LUT_B16(8'h80)    |                  |    |    |    |    |                    |    | -       |
| R54h  | DGC LUT84              | W/R | -          | DGC_LUT_B17(8'h88)    |                  |    |    |    |    |                    |    | -       |
| R55h  | DGC LUT85              | W/R | -          | DGC_LUT_B18(8'h90)    |                  |    |    |    |    |                    |    | -       |
| R56h  | DGC LUT86              | W/R | -          | DGC_LUT_B19(8'h98)    |                  |    |    |    |    |                    |    | -       |
| R57h  | DGC LUT87              | W/R | -          | DGC_LUT_B20(8'hA0)    |                  |    |    |    |    |                    |    | -       |
| R58h  | DGC LUT88              | W/R | -          | DGC_LUT_B21(8'hA8)    |                  |    |    |    |    |                    |    | -       |
| R59h  | DGC LUT89              | W/R | -          | DGC_LUT_B22(8'hB0)    |                  |    |    |    |    |                    |    | -       |
| R5Ah  | DGC LUT90              | W/R | -          | DGC_LUT_B23(8'hB8)    |                  |    |    |    |    |                    |    | -       |
| R5Bh  | DGC LUT91              | W/R | -          | DGC_LUT_B24(8'hC0)    |                  |    |    |    |    |                    |    | -       |
| R5Ch  | DGC LUT92              | W/R | -          | DGC_LUT_B25(8'hC8)    |                  |    |    |    |    |                    |    | -       |
| R5Dh  | DGC LUT93              | W/R | -          | DGC_LUT_B26(8'hD0)    |                  |    |    |    |    |                    |    | -       |
| R5Eh  | DGC LUT94              | W/R | -          | DGC_LUT_B27(8'hD8)    |                  |    |    |    |    |                    |    | -       |
| R5Fh  | DGC LUT95              | W/R | -          | DGC_LUT_B28(8'hE0)    |                  |    |    |    |    |                    |    | -       |
| R60h  | DGC LUT96              | W/R | -          | DGC_LUT_B29(8'hE8)    |                  |    |    |    |    |                    |    | -       |
| R61h  | DGC LUT97              | W/R | -          | DGC_LUT_B30(8'hF0)    |                  |    |    |    |    |                    |    | -       |
| R62h  | DGC LUT98              | W/R | -          | DGC_LUT_B31(8'hF8)    |                  |    |    |    |    |                    |    | -       |
| R63h  | DGC LUT99              | W/R | -          | DGC_LUT_B32(8'hFC)    |                  |    |    |    |    |                    |    | -       |
| C3    | CABC Control 5         | W/R | -          | BC_C TL(0)            | PWMDIV[2:0](000) |    |    | 1  | 1  | INPLUS (1)         | 1  | -       |
| C5    | CABC Control 6         | W/R | -          | PWM_PERIOD[7:0] (43d) |                  |    |    |    |    |                    |    | -       |
| C7    | CABC Control 7         | W/R | -          | DIM_FRAME[6:0] (20)   |                  |    |    |    |    |                    |    | -       |
| CB    | Gain select register 0 | W/R | -          | -                     | DBG0[6:0](40)    |    |    |    |    |                    | -  |         |
| CC    | Gain select register 1 | W/R | -          | -                     | DBG1[6:0](3C)    |    |    |    |    |                    | -  |         |
| CD    | Gain select register 2 | W/R | -          | -                     | DBG2[6:0](38)    |    |    |    |    |                    | -  |         |
| CE    | Gain select register 3 | W/R | -          | -                     | DBG3[6:0](34)    |    |    |    |    |                    | -  |         |
| CF    | Gain select register 4 | W/R | -          | -                     | DBG4[6:0](33)    |    |    |    |    |                    | -  |         |
| D0    | Gain select register 5 | W/R | -          | -                     | DBG5[6:0](32)    |    |    |    |    |                    | -  |         |
| D1    | Gain select register 6 | W/R | -          | -                     | DBG6[6:0](2B)    |    |    |    |    |                    | -  |         |
| D2    | Gain select register 7 | W/R | -          | -                     | DBG7[6:0](24)    |    |    |    |    |                    | -  |         |
| D3    | Gain select register 8 | W/R | -          | -                     | DBG8[6:0](22)    |    |    |    |    |                    | -  |         |
| FF    | Page select            | W/R | -          | -                     | -                | -  | -  | -  | -  | PAGE_SEL[1:0] (00) | -  |         |

Table 6.2: List table of command set page 1

**6.2 Index register**

| R/W | DNC | RB7 | RB6 | RB5 | RB4 | RB3 | RB2 | RB1 | RB0 |
|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|
| W   | 0   | ID7 | ID6 | ID5 | ID4 | ID3 | ID2 | ID1 | ID0 |
| R   | 0   | ID7 | ID6 | ID5 | ID4 | ID3 | ID2 | ID1 | ID0 |

Figure 6.1: Index register

Index register (IR) specifies the Index of register from R00h to RFFh. It sets the register number (ID7-0) in the range from 00000000b to 11111111b in binary form.

**6.3 Himax ID register (PAGE0 - R00h)**

| R/W | DNC | RB7 | RB6 | RB5 | RB4 | RB3 | RB2 | RB1 | RB0 |
|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|
| R   | 1   | 0   | 1   | 0   | 0   | 0   | 1   | 1   | 1   |

Figure 6.2: Himax ID register (PAGE0 -00h)

This command is used to read this IC’s ID code. The ID code of this IC is 75h.

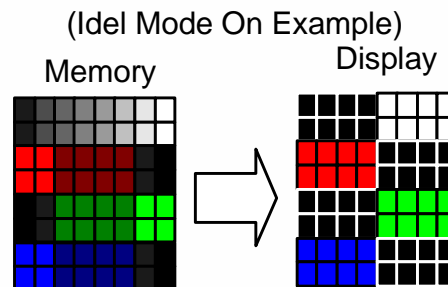
**6.4 Display mode control register (PAGE0 -01h)**

| R/W | DNC | RB7    | RB6      | RB5 | RB4 | RB3     | RB2    | RB1    | RB0    |
|-----|-----|--------|----------|-----|-----|---------|--------|--------|--------|
| W   | 1   | DP_STB | DP_STB_S | *   | *   | SCR_OLL | IDMO_N | INVO_N | PLT_ON |
| R   | 1   | DP_STB | DP_STB_S | 0   | 0   | SCR_OLL | IDMO_N | INVO_N | PLT_ON |

Figure 6.3: Display mode control register (PAGE0 -01h)

**DP\_STB, DP\_STB\_S** : These two bits can let the driver into the deep standby mode. And when into deep standby, all display operation stops, including the internal R-C oscillator. In the deep standby mode, the GRAM data and register content are not retained. For details, please refer to “5.11 Power On/Off Sequence” section for detailed use.

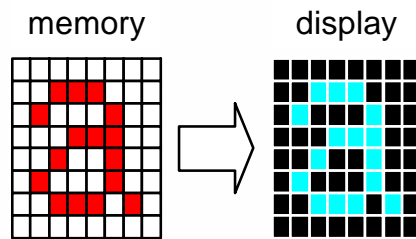
**IDMON**: This bit is Idle mode (8-color display mode) enable bit. **IDMON** = ‘1’, chip will be into idle mode, and color expression is reduced. The primary and the secondary colors using MSB of each R, G and B in the Frame Memory, 8 color depth data is displayed.



**SCROLL** : This bit turns on scroll mode by setting SCROLL = '1'. The scroll mode window is described by the Vertical Scroll Area command **TFA[15:0]**, **VSA[15:0]**, **BFA[15:0]** and the **Vertical start address VSP[15:0]** (R0Eh~R15h). To leave scroll mode to normal mode, the **SCROLL** bit should be set to '0'.

**INVON**: This bit is display inversion mode enable bit. **INVON** = '1', chip will be into display inversion mode, and makes no change of contents of frame memory. Every bit is inverted from the frame memory to the display.

(Example)



**PTLON**: This command is used for turning on/off Partial mode by setting PTLON=1/0. The Partial mode window is described by the Partial Area command **PSL[15:0]**, **PEL[15:0]** bits(R0Ah~R0Dh). To leave Partial mode to normal mode, the **PLTON** bit should be set to '0'.

**6.5 Column address start register (PAGE0 -02~03h)**

| R/W | DNC | RB7      | RB6      | RB5      | RB4      | RB3      | RB2      | RB1 | RB0 |
|-----|-----|----------|----------|----------|----------|----------|----------|-----|-----|
| W   | 1   | SC<br>15 | SC<br>14 | SC<br>13 | SC<br>12 | SC<br>11 | SC<br>10 | SC9 | SC8 |
| R   | 1   | SC<br>15 | SC<br>14 | SC<br>13 | SC<br>12 | SC<br>11 | SC<br>10 | SC9 | SC8 |

Figure 6.4: Column address start register upper byte (PAGE0 -02h)

| R/W | DNC | RB7 | RB6 | RB5 | RB4 | RB3 | RB2 | RB1 | RB0 |
|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|
| W   | 1   | SC7 | SC6 | SC5 | SC4 | SC3 | SC2 | SC1 | SC0 |
| R   | 1   | SC7 | SC6 | SC5 | SC4 | SC3 | SC2 | SC1 | SC0 |

Figure 6.5: Column address start register low byte (PAGE0 -03h)



**6.6 Column address end register (PAGE0 -04~05h)**

| R/W | DNC | RB7      | RB6      | RB5      | RB4      | RB3      | RB2      | RB1 | RB0 |
|-----|-----|----------|----------|----------|----------|----------|----------|-----|-----|
| W   | 1   | EC<br>15 | EC<br>14 | EC<br>13 | EC<br>12 | EC<br>11 | EC<br>10 | EC9 | EC8 |
| R   | 1   | EC<br>15 | EC<br>14 | EC<br>13 | EC<br>12 | EC<br>11 | EC<br>10 | EC9 | EC8 |

Figure 6.6: Column address end register upper byte (PAGE0 -04h)

| R/W | DNC | RB7 | RB6 | RB5 | RB4 | RB3 | RB2 | RB1 | RB0 |
|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|
| W   | 1   | EC7 | EC6 | EC5 | EC4 | EC3 | EC2 | EC1 | EC0 |
| R   | 1   | EC7 | EC6 | EC5 | EC4 | EC3 | EC2 | EC1 | EC0 |

Figure 6.7: Column address end register low byte (PAGE0 -05h)

**6.7 Row address start register (PAGE0 -06~07h)**

| R/W | DNC | RB7      | RB6      | RB5      | RB4      | RB3      | RB2      | RB1 | RB0 |
|-----|-----|----------|----------|----------|----------|----------|----------|-----|-----|
| W   | 1   | SP<br>15 | SP<br>14 | SP<br>13 | SP<br>12 | SP<br>11 | SP<br>10 | SP9 | SP8 |
| R   | 1   | SP<br>15 | SP<br>14 | SP<br>13 | SP<br>12 | SP<br>11 | SP<br>10 | SP9 | SP8 |

Figure 6.8: Row address start register upper byte (PAGE0 -06h)

| R/W | DNC | RB7 | RB6 | RB5 | RB4 | RB3 | RB2 | RB1 | RB0 |
|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|
| W   | 1   | SP7 | SP6 | SP5 | SP4 | SP3 | SP2 | SP1 | SP0 |
| R   | 1   | SP7 | SP6 | SP5 | SP4 | SP3 | SP2 | SP1 | SP0 |

Figure 6.9: Row address start register low byte (PAGE0 -07h)

**6.8 Row address end register (PAGE0 -08~09h)**

| R/W | DNC | RB7      | RB6      | RB5      | RB4      | RB3      | RB2      | RB1 | RB0 |
|-----|-----|----------|----------|----------|----------|----------|----------|-----|-----|
| W   | 1   | EP<br>15 | EP<br>14 | EP<br>13 | EP<br>12 | EP<br>11 | EP<br>10 | EP9 | EP8 |
| R   | 1   | EP<br>15 | EP<br>14 | EP<br>13 | EP<br>12 | EP<br>11 | EP<br>10 | EP9 | EP8 |

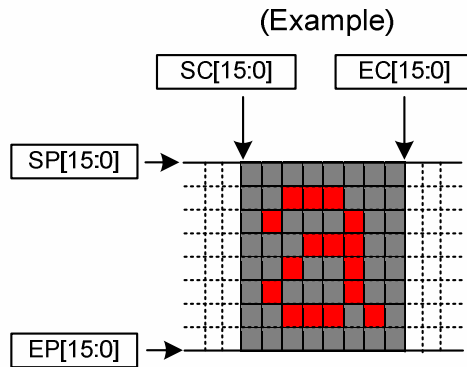
Figure 6.10: Row address end register upper byte (PAGE0 -08h)

| R/W | DNC | RB7 | RB6 | RB5 | RB4 | RB3 | RB2 | RB1 | RB0 |
|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|
| W   | 1   | EP7 | EP6 | EP5 | EP4 | EP3 | EP2 | EP1 | EP0 |
| R   | 1   | EP7 | EP6 | EP5 | EP4 | EP3 | EP2 | EP1 | EP0 |

Figure 6.11: Row address end register low byte (PAGE0 -09h)



These commands (R02h~R09h) are used to define area of frame memory where MCU can access. The values of SC[15:0], EC[15:0], SP[15:0] and EP[15:0] are referred when RAMWR command comes. Each value of SC[15:0], EC[15:0] represents one column line in the Frame Memory. Each value of SP[15:0], EP[15:0] represents one page line in the Frame Memory.



**6.9 Partial area start row register (PAGE0 -0A~0Bh)**

| R/W | DNC | RB7    | RB6    | RB5    | RB4    | RB3    | RB2    | RB1   | RB0   |
|-----|-----|--------|--------|--------|--------|--------|--------|-------|-------|
| W   | 1   | PSL 15 | PSL 14 | PSL 13 | PSL 12 | PSL 11 | PSL 10 | PSL 9 | PSL 8 |
| R   | 1   | PSL 15 | PSL 14 | PSL 13 | PSL 12 | PSL 11 | PSL 10 | PSL 9 | PSL 8 |

Figure 6.12: Partial area start row register upper byte (PAGE0 -0Ah)

| R/W | DNC | RB7   | RB6   | RB5   | RB4   | RB3   | RB2   | RB1   | RB0   |
|-----|-----|-------|-------|-------|-------|-------|-------|-------|-------|
| W   | 1   | PSL 7 | PSL 6 | PSL 5 | PSL 4 | PSL 3 | PSL 2 | PSL 1 | PSL 0 |
| R   | 1   | PSL 7 | PSL 6 | PSL 5 | PSL 4 | PSL 3 | PSL 2 | PSL 1 | PSL 0 |

Figure 6.13: Partial area start row register low byte (PAGE0 -0Bh)

**6.10 Partial area end row register (PAGE0 -0C~0Dh)**

| R/W | DNC | RB7    | RB6    | RB5    | RB4    | RB3    | RB2    | RB1   | RB0   |
|-----|-----|--------|--------|--------|--------|--------|--------|-------|-------|
| W   | 1   | PEL 15 | PEL 14 | PEL 13 | PEL 12 | PEL 11 | PEL 10 | PEL 9 | PEL 8 |
| R   | 1   | PEL 15 | PEL 14 | PEL 13 | PEL 12 | PEL 11 | PEL 10 | PEL 9 | PEL 8 |

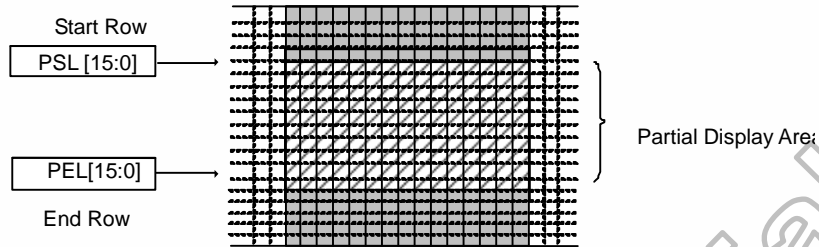
Figure 6.14: Partial area end row register upper byte (PAGE0 -0Ch)

| R/W | DNC | RB7   | RB6   | RB5   | RB4   | RB3   | RB2   | RB1   | RB0   |
|-----|-----|-------|-------|-------|-------|-------|-------|-------|-------|
| W   | 1   | PEL 7 | PEL 6 | PEL 5 | PEL 4 | PEL 3 | PEL 2 | PEL 1 | PEL 0 |
| R   | 1   | PEL 7 | PEL 6 | PEL 5 | PEL 4 | PEL 3 | PEL 2 | PEL 1 | PEL 0 |

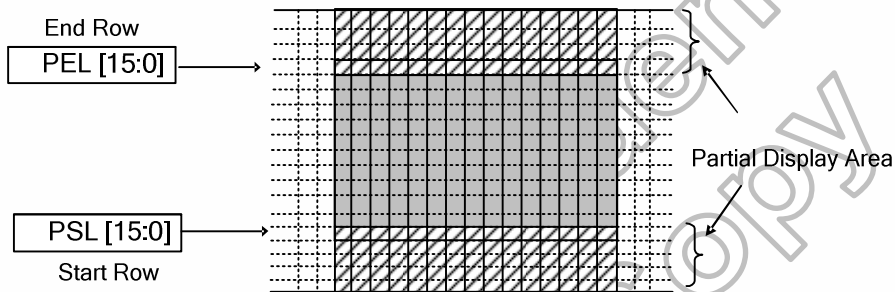
Figure 6.15: Partial area end row register low byte (PAGE0 -0Dh)

These commands (PAGE0 -0Ah~~0Dh) define the partial mode's display area. The Start Row (PSL) and the second the End Row (PEL) are illustrated in the figures below. PSL and PEL refer to the Frame Memory Line Pointer.

If End Row > Start Row



If End Row < Start Row



If End Row = Start Row then the Partial Area will be one row deep.

**6.11 Vertical scroll top fixed area register (PAGE0 -0E~0Fh)**

| R/W | DNC | RB7       | RB6       | RB5       | RB4       | RB3       | RB2       | RB1      | RB0      |
|-----|-----|-----------|-----------|-----------|-----------|-----------|-----------|----------|----------|
| W   | 1   | TFA<br>15 | TFA<br>14 | TFA<br>13 | TFA<br>12 | TFA<br>11 | TFA<br>10 | TFA<br>9 | TFA<br>8 |
| R   | 1   | TFA<br>15 | TFA<br>14 | TFA<br>13 | TFA<br>12 | TFA<br>11 | TFA<br>10 | TFA<br>9 | TFA<br>8 |

Figure 6.16: Vertical scroll top fixed area register upper byte (PAGE0 -0Eh)

| R/W | DNC | RB7      | RB6      | RB5      | RB4      | RB3      | RB2      | RB1      | RB0      |
|-----|-----|----------|----------|----------|----------|----------|----------|----------|----------|
| W   | 1   | TFA<br>7 | TFA<br>6 | TFA<br>5 | TFA<br>4 | TFA<br>3 | TFA<br>2 | TFA<br>1 | TFA<br>0 |
| R   | 1   | TFA<br>7 | TFA<br>6 | TFA<br>5 | TFA<br>4 | TFA<br>3 | TFA<br>2 | TFA<br>1 | TFA<br>0 |

Figure 6.17: Vertical scroll top fixed area register low byte (PAGE0 -0Fh)

**6.12 Vertical scroll height area register (PAGE0 -10~11h)**

| R/W | DNC | RB7       | RB6       | RB5       | RB4       | RB3       | RB2       | RB1      | RB0      |
|-----|-----|-----------|-----------|-----------|-----------|-----------|-----------|----------|----------|
| W   | 1   | VSA<br>15 | VSA<br>14 | VSA<br>13 | VSA<br>12 | VSA<br>11 | VSA<br>10 | VSA<br>9 | VSA<br>8 |
| R   | 1   | VSA<br>15 | VSA<br>14 | VSA<br>13 | VSA<br>12 | VSA<br>11 | VSA<br>10 | VSA<br>9 | VSA<br>8 |

Figure 6.18: Vertical scroll height area register upper byte (PAGE0 -10h)

| R/W | DNC | RB7      | RB6      | RB5      | RB4      | RB3      | RB2      | RB1      | RB0      |
|-----|-----|----------|----------|----------|----------|----------|----------|----------|----------|
| W   | 1   | VSA<br>7 | VSA<br>6 | VSA<br>5 | VSA<br>4 | VSA<br>3 | VSA<br>2 | VSA<br>1 | VSA<br>0 |
| R   | 1   | VSA<br>7 | VSA<br>6 | VSA<br>5 | VSA<br>4 | VSA<br>3 | VSA<br>2 | VSA<br>1 | VSA<br>0 |

Figure 6.19: Vertical scroll height area register low byte (PAGE0 -11h)

**6.13 Vertical scroll button fixed area register (PAGE0 -12~13h)**

| R/W | DNC | RB7       | RB6       | RB5       | RB4       | RB3       | RB2       | RB1      | RB0      |
|-----|-----|-----------|-----------|-----------|-----------|-----------|-----------|----------|----------|
| W   | 1   | BFA<br>15 | BFA<br>14 | BFA<br>13 | BFA<br>12 | BFA<br>11 | BFA<br>10 | BFA<br>9 | BFA<br>8 |
| R   | 1   | BFA<br>15 | BFA<br>14 | BFA<br>13 | BFA<br>12 | BFA<br>11 | BFA<br>10 | BFA<br>9 | BFA<br>8 |

Figure 6.20: Vertical scroll button fixed area register upper byte (PAGE0 -12h)

| R/W | DNC | RB7      | RB6      | RB5      | RB4      | RB3      | RB2      | RB1      | RB0      |
|-----|-----|----------|----------|----------|----------|----------|----------|----------|----------|
| W   | 1   | BFA<br>7 | BFA<br>6 | BFA<br>5 | BFA<br>4 | BFA<br>3 | BFA<br>2 | BFA<br>1 | BFA<br>0 |
| R   | 1   | BFA<br>7 | BFA<br>6 | BFA<br>5 | BFA<br>4 | BFA<br>3 | BFA<br>2 | BFA<br>1 | BFA<br>0 |

Figure 6.21: Vertical scroll button fixed area register low byte (PAGE0 -13h)

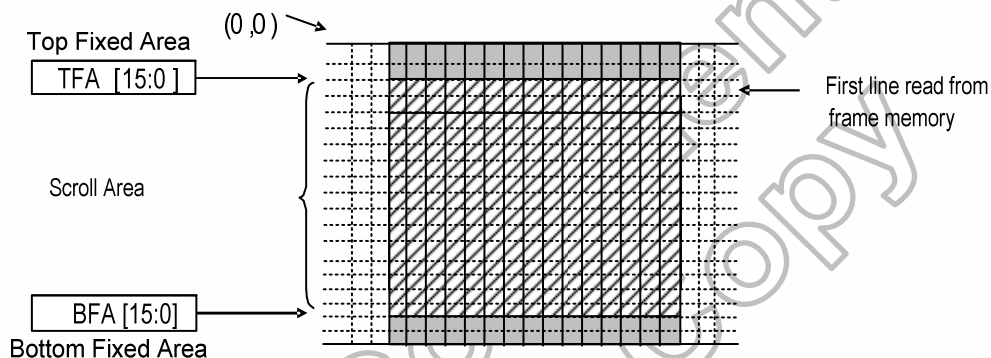
These commands (PAGE0 -0E~0Fh, R10~11h, R12~13h) define the Vertical Scrolling Area of the display.

**TFA[15:0]** describes the Top Fixed Area (in No. of lines from Top of the Frame Memory and Display).

**VSA[15:0]** describes the height of the Vertical Scrolling Area (in No. of lines of the Frame Memory [not the display] from the Vertical Scrolling Start Address). The first line read from Frame Memory appears immediately after the bottom most line of the Top Fixed Area.

**BFA[15:0]** describes the Bottom Fixed Area (in No. of lines from Bottom of the Frame Memory and Display).

TFA, VSA and BFA refer to the Frame Memory Line Pointer.



Please note that (TFA+VSA+BFA) must be set to '320d', otherwise Scrolling mode is undefined. In Vertical Scroll Mode, **MV** bit should be set to '0' – this only affects the Frame Memory Write.

**6.14 Vertical scroll start address register (PAGE0 -14~15h)**

| R/W | DNC | RB7       | RB6       | RB5       | RB4       | RB3       | RB2       | RB1      | RB0      |
|-----|-----|-----------|-----------|-----------|-----------|-----------|-----------|----------|----------|
| W   | 1   | VSP<br>15 | VSP<br>14 | VSP<br>13 | VSP<br>12 | VSP<br>11 | VSP<br>10 | VSP<br>9 | VSP<br>8 |
| R   | 1   | VSP<br>15 | VSP<br>14 | VSP<br>13 | VSP<br>12 | VSP<br>11 | VSP<br>10 | VSP<br>9 | VSP<br>8 |

Figure 6.22: Vertical scroll start address register upper byte (PAGE0 -14h)

| R/W | DNC | RB7      | RB6      | RB5      | RB4      | RB3      | RB2      | RB1      | RB0      |
|-----|-----|----------|----------|----------|----------|----------|----------|----------|----------|
| W   | 1   | VSP<br>7 | VSP<br>6 | VSP<br>5 | VSP<br>4 | VSP<br>3 | VSP<br>2 | VSP<br>1 | VSP<br>0 |
| R   | 1   | VSP<br>7 | VSP<br>6 | VSP<br>5 | VSP<br>4 | VSP<br>3 | VSP<br>2 | VSP<br>1 | VSP<br>0 |

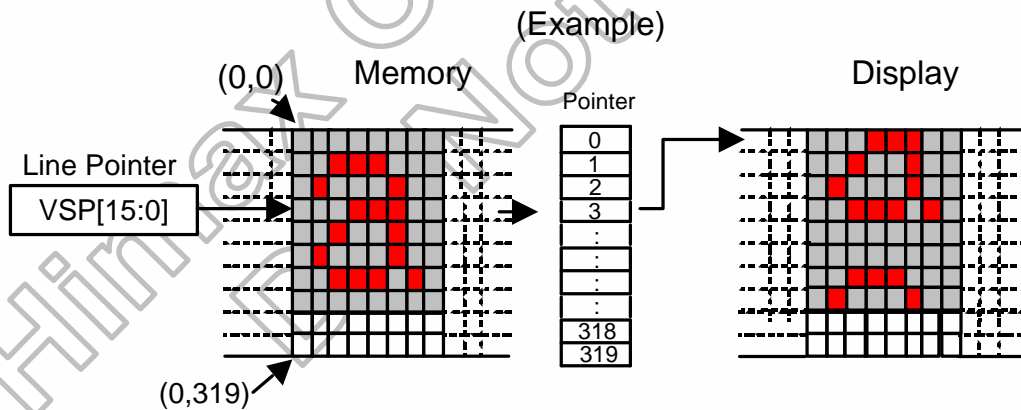
Figure 6.23: Vertical scroll start address register low byte (PAGE0 -15h)

**VSP[15:0]** is used together with Vertical Scrolling Definition register (PAGE0 -0Eh~R13h), which describe the scrolling area and the scrolling mode.

**VSP[15:0]** refers to the Frame Memory line Pointer, and describes the address of the line in the Frame Memory that will be written as the first line after the last line of the Top Fixed Area on the display as illustrated below:

Example:

When Top Fixed Area TFA = '00d', Bottom Fixed Area BFA = '02'd, Vertical Scrolling Area VSA = '318'd and VSP = '3d' (**SS\_Panel** = '0', **GS\_Panel** = '0')



When new Pointer position and Picture Data are sent, the result on the display will happen at the next Panel Scan to avoid tearing effect.

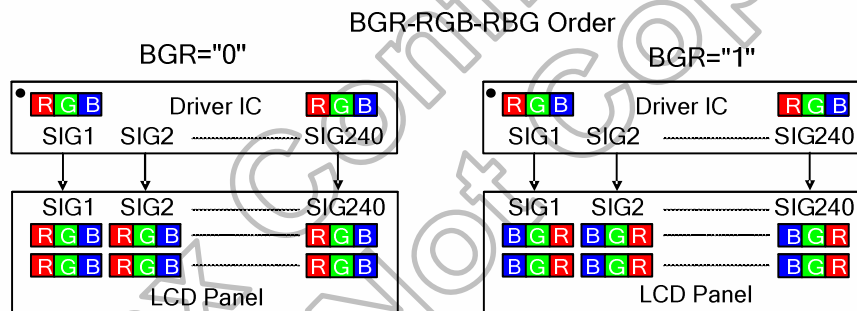
**6.15 Memory access control register (PAGE0 -16h)**

|           |            |     |     |     |     |     |     |     |     |
|-----------|------------|-----|-----|-----|-----|-----|-----|-----|-----|
| <b>RW</b> | <b>DNC</b> | RB7 | RB6 | RB5 | RB4 | RB3 | RB2 | RB1 | RB0 |
| <b>W</b>  | <b>1</b>   | MY  | MX  | MV  | ML  | BGR | *   | *   | *   |
| <b>R</b>  | <b>1</b>   | MY  | MX  | MV  | ML  | BGR | 0   | 0   | 0   |

**Figure 6.24: Memory access control register (PAGE0 -16h)**

This command defines read/write scanning direction of frame memory. **MX**, **MY** bits also define the display direction in the RGB interface. This command makes no change on the other driver status. For details, please refer to “5.2.1 System interface to GRAM Write Direction” section.

| Bit | Name                  | Description  |
|-----|-----------------------|--|
| MY  | PAGE ADDRESS ORDER    | These 3 bits controls MCU to memory write/read direction. “MCU to memory write/read direction” |
| MX  | COLUMN ADDRESS ORDER  |  |
| MV  | PAGE/COLUMN SELECTION |  |
| ML  | Vertical ORDER        | LCD vertical refresh direction control   |
| BGR | RGB-BGR ORDER         | Color selector switch control (0=RGB color filter panel, 1=BGR color filter panel)             |



**6.16 COLMOD control register (PAGE0 -17h)**

|            |            |       |       |       |       |     |       |       |       |
|------------|------------|-------|-------|-------|-------|-----|-------|-------|-------|
| <b>R/W</b> | <b>DNC</b> | RB7   | RB6   | RB5   | RB4   | RB3 | RB2   | RB1   | RB0   |
| <b>W</b>   | <b>1</b>   | CSEL3 | CSEL2 | CSEL1 | CSEL0 | *   | IFPF2 | IFPF1 | IFPF0 |
| <b>R</b>   | <b>1</b>   | CSEL3 | CSEL2 | CSEL1 | CSEL0 | *   | IFPF2 | IFPF1 | IFPF0 |

**Figure 6.25: COLMOD control register (PAGE0 -17h)**

This command is used to define the format of RGB picture data, which is to be transfer via the system and RGB interface. The formats are shown in the table:

**System interface**

| Interface Format                                  | IFPF2 | IFPF1 | IFPF0 |
|---|-------|-------|-------|
| Not Defined                                       | 0     | 0     | 0     |
| Not Defined                                       | 0     | 0     | 1     |
| Not Defined                                       | 0     | 1     | 0     |
| 12 Bit/Pixel                                      | 0     | 1     | 1     |
| Not Defined                                       | 1     | 0     | 0     |
| 16 Bit/Pixel                                      | 1     | 0     | 1     |
| 18 Bit/Pixel                                      | 1     | 1     | 0     |
| 18 Bit/Pixel at 16-bits data bus interface (16+2) | 1     | 1     | 1     |

**RGB interface**

| Interface Format | CSEL3             | CSEL2 | CSEL1 | CSEL0 |
|------------------|-------------------|-------|-------|-------|
| 16 Bit/Pixel     | 0                 | 1     | 0     | 1     |
| 18 Bit/Pixel     | 0                 | 1     | 1     | 0     |
| 6 Bit/Pixel      | 1                 | 1     | 1     | 0     |
| Not Defined      | The Other Setting |       |       |       |



**6.17 OSC control register (PAGE0 -18h & R19h)**

|            |            |               |               |              |               |               |               |               |               |
|------------|------------|---------------|---------------|--------------|---------------|---------------|---------------|---------------|---------------|
| <b>R/W</b> | <b>DNC</b> | RB7           | RB6           | RB5          | RB4           | RB3           | RB2           | RB1           | RB0           |
| <b>W</b>   | <b>1</b>   | I/P_R<br>ADJ3 | I/P_R<br>ADJ2 | IP_RA<br>DJ1 | I/P_R<br>ADJ0 | N/P_R<br>ADJ3 | N/P_R<br>ADJ2 | N/P_R<br>ADJ1 | N/P_R<br>ADJ0 |
| <b>R</b>   | <b>1</b>   | I/P_R<br>ADJ3 | I/P_R<br>ADJ2 | IP_RA<br>DJ1 | I/P_R<br>ADJ0 | N/P_R<br>ADJ3 | N/P_R<br>ADJ2 | N/P_R<br>ADJ1 | N/P_R<br>ADJ0 |

Figure 6.26: OSC control 1 register (PAGE0 -18h)

|            |            |     |     |     |     |     |     |     |        |
|------------|------------|-----|-----|-----|-----|-----|-----|-----|--------|
| <b>R/W</b> | <b>DNC</b> | RB7 | RB6 | RB5 | RB4 | RB3 | RB2 | RB1 | RB0    |
| <b>W</b>   | <b>1</b>   | *   | *   | *   | *   | *   | *   | *   | OSC_EN |
| <b>R</b>   | <b>1</b>   | 0   | 0   | 0   | 0   | 0   | 0   | 0   | OSC_EN |

Figure 6.27: OSC control 2 register (PAGE0 -19h)

These commands are used to set internal oscillator related setting

**OSC\_EN:** Enable internal oscillator, OSC\_EN = '1', internal oscillator start to oscillate. OSC\_EN = '0', internal oscillator stop. In RGB interface mode (PAGE0 -RCM[1:0] = '10' or '11'), internal oscillator will be stop to oscillate and OSC\_EN bit control is invalid.

**N/P\_RADJ[2:0]:** Internal oscillator frequency adjusts in Normal / Partial mode.

**I/PI\_RADJ[2:0]:** Internal oscillator frequency adjusts in Idle(8-color) / Partial Idle mode.

For details, please refer to "5.5 Oscillator" section.

| RADJ3 | RADJ2 | RADJ1 | RADJ0 | Internal Oscillator Frequency | Display Frame rate |
|-------|-------|-------|-------|-------------------------------|--------------------|
| 0     | 0     | 0     | 0     | 50% x 2.75MHz                 | 30Hz               |
| 0     | 0     | 0     | 1     | 67% x 2.75MHz                 | 40Hz               |
| 0     | 0     | 1     | 0     | 75% x 2.75MHz                 | 45Hz               |
| 0     | 0     | 1     | 1     | 83% x 2.75MHz                 | 50Hz               |
| 0     | 1     | 0     | 0     | 100% x2.75MHz                 | 60Hz               |
| 0     | 1     | 0     | 1     | 108% x 2.75MHz                | 65Hz               |
| 0     | 1     | 1     | 0     | 117% x 2.75MHz                | 70Hz               |
| 0     | 1     | 1     | 1     | 125% x 2.75MHz                | 75Hz               |
| 1     | 0     | 0     | 0     | 100% x 2.75MHz                | 60Hz               |
| 1     | 0     | 0     | 1     | 133% x 2.75MHz                | 80Hz               |
| 1     | 0     | 1     | 0     | 150% x 2.75MHz                | 90Hz               |
| 1     | 0     | 1     | 1     | 167% x 2.75MHz                | 100Hz              |
| 1     | 1     | 0     | 0     | 200% x 2.75MHz                | 120Hz              |
| 1     | 1     | 0     | 1     | 217% x 2.75MHz                | 130Hz              |
| 1     | 1     | 1     | 0     | 233% x 2.75MHz                | 140Hz              |
| 1     | 1     | 1     | 1     | 250% x 2.75MHz                | 150Hz              |

## 6.18 Power control 1 register (PAGE0 -1Ah)

| R/W | DNC | RB7 | RB6 | RB5 | RB4 | RB3 | RB2 | RB1 | RB0 |
|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|
| W   | 1   | *   | *   | *   | *   | *   | BT2 | BT1 | BT0 |
| R   | 1   | *   | *   | *   | *   | *   | BT2 | BT0 | BT0 |

Figure 6.28: Power control 1 register (PAGE0 -1Ah)

**BT[2:0]:** Switch the output factor of step-up circuit 2 for VGH and VGL voltage generation. The LCD drive voltage level can be selected according to the characteristic of liquid crystal which panel used. Lower amplification of the step-up circuit consumes less current and then the power consumption can be reduced.

| BT2 | BT1 | BT0 | DDVDH | VCL  | VGH        | VGL         |
|-----|-----|-----|-------|------|------------|-------------|
| 0   | 0   | 0   | 5.0V  | -VCI | 3DDVDH     | -VCI-2DDVDH |
| 0   | 0   | 1   | 5.0V  | -VCI | 3DDVDH     | -2DDVDH     |
| 0   | 1   | 0   | 5.0V  | -VCI | 3DDVDH     | VCI-2DDVDH  |
| 0   | 1   | 1   | 5.0V  | -VCI | VCI+2DDVDH | -VCI-2DDVDH |
| 1   | 0   | 0   | 5.0V  | -VCI | VCI+2DDVDH | -2DDVDH     |
| 1   | 0   | 1   | 5.0V  | -VCI | VCI+2DDVDH | VCI-2DDVDH  |
| 1   | 1   | 0   | 5.0V  | -VCI | 2DDVDH     | -2DDVDH     |
| 1   | 1   | 1   | 5.0V  | -VCI | 2DDVDH     | -VCI-DDVDH  |

Note: When VCI = 2.8V, DDVDH\_TRI=0

| BT2 | BT1 | BT0 | DDVDH | VCL  | VGH               | VGL               |
|-----|-----|-----|-------|------|-------------------|-------------------|
| 0   | 0   | 0   | 6.1V  | -VCI | Setting inhabited | Setting inhabited |
| 0   | 0   | 1   | 6.1V  | -VCI | 3DDVDH            | -2DDVDH           |
| 0   | 1   | 0   | 6.1V  | -VCI | 3DDVDH            | VCI-2DDVDH        |
| 0   | 1   | 1   | 6.1V  | -VCI | VCI+2DDVDH        | -VCI-2DDVDH       |
| 1   | 0   | 0   | 6.1V  | -VCI | VCI+2DDVDH        | -2DDVDH           |
| 1   | 0   | 1   | 6.1V  | -VCI | VCI+2DDVDH        | VCI-2DDVDH        |
| 1   | 1   | 0   | 6.1V  | -VCI | 2DDVDH            | -2DDVDH           |
| 1   | 1   | 1   | 6.1V  | -VCI | 2DDVDH            | -VCI-DDVDH        |

Note: When VCI = 2.8V, DDVDH\_TRI=1

6.19 Power control 2 register (PAGE0 -1Bh)

|     |     |     |     |      |      |      |      |      |      |
|-----|-----|-----|-----|------|------|------|------|------|------|
| R/W | DNC | RB7 | RB6 | RB5  | RB4  | RB3  | RB2  | RB1  | RB0  |
| W   | 1   | *   | *   | VRH5 | VRH4 | VRH3 | VRH2 | VRH1 | VRH0 |
| R   | 1   | *   | *   | VRH5 | VRH4 | VRH3 | VRH2 | VRH1 | VRH0 |

Figure 6.29: Power control 2 register (PAGE0 -1Bh)

VRH[4:0]: Specify the VREG1 voltage adjusting. VREG1 voltage is for gamma voltage setting.  $VREG1 = \text{Decimal}(VRH[5:0]) \times 0.05 + 3.3$ .

| VRH5 | VRH4 | VRH3 | VRH2 | VRH1 | VRH0 | VREG1 (DDVDH_TRI=0)  | VREG1 (DDVDH_TRI=1) |
|------|------|------|------|------|------|--|---------------------|
| 0    | 0    | 0    | 0    | 0    | 0    | 3.30   | 3.30                |
| 0    | 0    | 0    | 0    | 0    | 1    | 3.35   | 3.35                |
| 0    | 0    | 0    | 0    | 1    | 0    | 3.40   | 3.40                |
| 0    | 0    | 0    | 0    | 1    | 1    | 3.45   | 3.45                |
| 0    | 0    | 0    | 1    | 0    | 0    | 3.50   | 3.50                |
| 0    | 0    | 0    | 1    | 0    | 1    | 3.55   | 3.55                |
| 0    | 0    | 0    | 1    | 1    | 0    | 3.60   | 3.60                |
| 0    | 0    | 0    | 1    | 1    | 1    | 3.65   | 3.65                |
| 0    | 0    | 1    | 0    | 0    | 0    | 3.70   | 3.70                |
| :    | :    | :    | :    | :    | :    | :  | :                   |
| 0    | 1    | 1    | 1    | 0    | 1    | 4.75   | 4.75                |
| 0    | 1    | 1    | 1    | 1    | 0    | 4.80   | 4.80                |
| 0    | 1    | 1    | 1    | 1    | 1    | STOP   | 4.85                |
| 1    | 0    | 0    | 0    | 0    | 0    | STOP   | 4.90                |
| 1    | 0    | 0    | 0    | 0    | 1    | STOP   | 4.95                |
| :    | :    | :    | :    | :    | :    | :  | :                   |
| 1    | 1    | 0    | 0    | 0    | 0    | STOP   | 5.70                |
| 1    | 1    | 0    | 0    | 0    | 1    | STOP   | 5.75                |
| 1    | 1    | 0    | 0    | 1    | 0    | STOP   | 5.80                |
| 1    | 1    | 0    | 0    | 1    | 1    | STOP   | STOP                |
| 1    | 1    | 1    | 0    | 1    | 1    | STOP   | STOP                |
| :    | :    | :    | :    | :    | :    | :  | :                   |
| 1    | 1    | 1    | 1    | 1    | 0    | STOP   | STOP                |
| 1    | 1    | 1    | 1    | 1    | 1    | Internal circuit operations stop. The gamma voltage can be adjusted from external VREG1 input. |                     |

Note: Internal VREF can be modified by Custom' s special request. default VREF=4.8 if

DDVDH\_TRI=0 and VREF=5.8 if DDVDH\_TRI=1

$VREG1 = \{\text{Decimal}(VRH[5:0]) \times 0.05 + 3.3\} \times (VREF / 4.8)$  if DDVDH\_TRI=0.

$VREG1 = \{\text{Decimal}(VRH[5:0]) \times 0.05 + 3.3\} \times (VREF / 5.8)$  if DDVDH\_TRI=1.

**6.20 Power control 3 register (PAGE0 -1Ch)**

| R/W | DNC | RB7 | RB6 | RB5 | RB4 | RB3 | RB2 | RB1 | RB0 |
|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|
| W   | 1   | *   | *   | *   | *   | *   | AP2 | AP1 | AP0 |
| R   | 1   | *   | *   | *   | *   | *   | AP2 | AP1 | AP0 |

Figure 6.30: Power control 3 register (PAGE0 -1Ch)

**AP[2:0]:** Adjust the amount of current driving for the operational amplifier in the power supply circuit. When the amount of fixed current is increased, the LCD driving capacity and the display quality are high, but the current consumption is increased. Adjust the fixed current by considering both the display quality and the current consumption.

| AP2 | AP1 | AP0 | Constant Current of Operational Amplifier    |
|-----|-----|-----|--|
| 0   | 0   | 0   | Operation of the operational amplifier stops |
| 0   | 0   | 1   | Small  |
| 0   | 1   | 0   | Small  |
| 0   | 1   | 1   | Small  |
| 1   | 0   | 0   | Medium                                       |
| 1   | 0   | 1   | Medium High                                  |
| 1   | 1   | 0   | Large  |
| 1   | 1   | 1   | Setting Inhibited                            |

**6.21 Power control 4 register (PAGE0 -1Dh)**

| R/W | DNC | RB7 | RB6           | RB5           | RB4           | RB3 | RB2          | RB1          | RB0          |
|-----|-----|-----|---------------|---------------|---------------|-----|--------------|--------------|--------------|
| W   | 1   | *   | I/PI_F<br>S02 | I/PI_F<br>S01 | I/PI_F<br>S00 | *   | N/P_<br>FS02 | N/P_<br>FS01 | N/P_<br>FS00 |
| R   | 1   | *   | I/PI_F<br>S02 | I/PI_F<br>S01 | I/PI_F<br>S00 | *   | N/P_<br>FS02 | N/P_<br>FS01 | N/P_<br>FS00 |

Figure 6.31: Power control 4 register (PAGE0 -1Dh)

**N/P\_FS0[2:0]:** Set the operating frequency of the step-up circuit 1 and extra step-up circuit 1 for DDVDH voltage generation in Normal / Partial mode.

**I/PI\_FS0[2:0]:** Set the operating frequency of the step-up circuit 1 and extra step-up circuit 1 for DDVDH voltage generation in Idle(8-color) / Partial Idle mode.

For details, please refer to “5.5 Oscillator” section.

| FS02 | FS01 | FS00 | Operation Frequency of Step-up Circuit 1 and Extra Step-up Circuit 1 |
|------|------|------|--|
| 0    | 0    | 0    | ¼ x H Line Frequency   |
| 0    | 0    | 1    | ½ x H Line Frequency   |
| 0    | 1    | 0    | 1 x H Line Frequency   |
| 0    | 1    | 1    | 1.5 x H Line Frequency   |
| 1    | 0    | 0    | 2 x H Line Frequency   |
| 1    | 0    | 1    | 3 x H Line Frequency   |
| 1    | 1    | 0    | 4 x H Line Frequency   |
| 1    | 1    | 1    | 8 x H Line Frequency   |

**6.22 Power control 5 register (PAGE0 -1Eh)**

| R/W | DNC | RB7 | RB6        | RB5        | RB4        | RB3 | RB2      | RB1      | RB0      |
|-----|-----|-----|------------|------------|------------|-----|----------|----------|----------|
| W   | 1   | *   | I/PI_F S12 | I/PI_F S11 | I/PI_F S10 | *   | N/P_FS12 | N/P_FS11 | N/P_FS10 |
| R   | 1   | *   | I/PI_F S12 | I/PI_F S11 | I/PI_F S10 | *   | N/P_FS12 | N/P_FS11 | N/P_FS10 |

Figure 6.32: Power control 5 register (PAGE0 -1Eh)

**N/P\_FS1[2:0]:** Set the operating frequency of the step-up circuit 2 and 3 for VGH, VGL and VCL voltage generation in Normal / Partial mode.

**I/PI\_FS1[2:0]:** Set the operating frequency of the step-up circuit 2 and 3 for VGH, VGL and VCL voltage generation in Idle(8-color) / Partial Idle mode.

For details, please refer to “5.5 Oscillator” section.

| FS12 | FS11 | FS10 | Operation Frequency of Step-up Circuit 2 , Step-up Circuit 3 |
|------|------|------|--|
| 0    | 0    | 0    | ¼ x H Line Frequency   |
| 0    | 0    | 1    | ½ x H Line Frequency   |
| 0    | 1    | 0    | 1 x H Line Frequency   |
| 0    | 1    | 1    | 1.5 x H Line Frequency                                       |
| 1    | 0    | 0    | 2 x H Line Frequency   |
| 1    | 0    | 1    | 3 x H Line Frequency   |
| 1    | 1    | 0    | 4 x H Line Frequency   |
| 1    | 1    | 1    | 8 x H Line Frequency   |

**Note:** Ensure that the operation frequency of step-up circuit 1 ≥ step-up circuit 2

**6.23 Power control 6 register (PAGE0 -1Fh)**

|           |            |        |        |     |     |     |     |             |     |
|-----------|------------|--------|--------|-----|-----|-----|-----|-------------|-----|
| <b>RW</b> | <b>DNC</b> | RB7    | RB6    | RB5 | RB4 | RB3 | RB2 | RB1         | RB0 |
| <b>W</b>  | <b>1</b>   | GAS EN | VCO MG | *   | PON | DK  | XDK | DDV DH_T RI | STB |
| <b>R</b>  | <b>1</b>   | GAS EN | VCO MG | *   | PON | DK  | XDK | DDV DH_T RI | STB |

Figure 6.33: Power control 6 register (PAGE0 -1Fh)

**PON:** Specify on/off control of step-up circuit 2 for VCL, VGL voltage generation. For detail, see the Power On/Off Setting Flow.

| PON | Operation of Step-up Circuit 2 |
|-----|--------------------------------|
| 0   | OFF                            |
| 1   | ON                             |

**DK:** Specify on/off control of step-up circuit 1 for DDVDH voltage generation. For detail, see the Power Supply Setting Sequence.

| DK | Operation of Step-up Circuit 1 |
|----|--------------------------------|
| 0  | ON                             |
| 1  | OFF                            |

**STB:** When **STB** = '1', the HX8347-G into the standby mode, where all display operations stop, suspend all the internal operations including the internal R-C oscillator. During the standby mode, only the following process can be executed. For details, please refer to STB mode flow.

- a. Start the oscillation
- b. Exit the Standby mode (STB = "0") ,

In the standby mode, the GRAM data and register content are retained.

**XDK, DDVDH\_TRI:** Specify the ratio of step-up circuit for DDVDH voltage generation.

| DDVDH_TRI | XDK | Step-up Circuit 1 | Capacitor Connection Pins Used |
|-----------|-----|-------------------|--------------------------------|
| 0         | 0   | 2 x VCI           | C11P, C11N                     |
| 0         | 1   | 2 x VCI           | C11P, C11N, C12P, C12N         |
| 1         | 0   | 3 x VCI           | C11P, C11N, C12P, C12N         |
| 1         | 1   | Setting inhabited | Setting inhabited              |

**VCOMG:** When **VCOMG** = '1', VCOML voltage can output to negative voltage (1.0V ~ VCL+0.5V). When **VCOMG** = '0', VCOML outputs GND and **VML[7:0]** setting are invalid. Then, low power consumption is accomplished.

**GASEN:** This stands for abnormal power-off monitor function when the power is off.

**6.24 Read data register (PAGE0 -22h)**

| R/W | RS | RB17     | RB16     | RB15     | RB14     | RB13     | RB12     | RB11     | RB10     | RB9     | RB8     | RB7     | RB6     | RB5     | RB4     | RB3     | RB2     | RB1     | RB0     |
|-----|----|----------|----------|----------|----------|----------|----------|----------|----------|---------|---------|---------|---------|---------|---------|---------|---------|---------|---------|
| W   | 1  | WD<br>17 | WD<br>16 | WD<br>15 | WD<br>14 | WD<br>13 | WD<br>12 | WD<br>11 | WD<br>10 | WD<br>9 | WD<br>8 | WD<br>7 | WD<br>6 | WD<br>5 | WD<br>4 | WD<br>3 | WD<br>2 | WD<br>1 | WD<br>0 |
| R   | 1  | RD<br>17 | RD<br>16 | RD<br>15 | RD<br>14 | RD<br>13 | RD<br>12 | RD<br>11 | RD<br>10 | RD<br>9 | RD<br>8 | RD<br>7 | RD<br>6 | RD<br>5 | RD<br>4 | RD<br>3 | RD<br>2 | RD<br>1 | RD<br>0 |

**Figure 6.34: Read data register (PAGE0 -22h)**

**WD[17:0]** : Transforms the data into 18-bit bus before written to GRAM through the write data register (WDR). After a write operation is issued, the address is automatically updated according to the AM and I/D bits.

**RD[17:0]**: Read 18-bit data from GRAM through the read data register (RDR). When the data is read by microcomputer, the first-word read immediately after the GRAM address setting is latched from the GRAM to the internal read-data latch. The data on the data bus (D17-0) becomes invalid and the second-word read is normal.

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**6.25 VCOM control 1~3 register (PAGE0 -23~25h)**

| R/W | DNC | RB7      | RB6      | RB5      | RB4      | RB3      | RB2      | RB1      | RB0      |
|-----|-----|----------|----------|----------|----------|----------|----------|----------|----------|
| W   | 1   | VMF<br>7 | VMF<br>6 | VMF<br>5 | VMF<br>4 | VMF<br>3 | VMF<br>2 | VMF<br>1 | VMF<br>0 |
| R   | 1   | VMF<br>7 | VMF<br>6 | VMF<br>5 | VMF<br>4 | VMF<br>3 | VMF<br>2 | VMF<br>1 | VMF<br>0 |

Figure 6.35: Vcom control 1 register (PAGE0 -23h)

| R/W | DNC | RB7      | RB6      | RB5      | RB4      | RB3      | RB2      | RB1      | RB0      |
|-----|-----|----------|----------|----------|----------|----------|----------|----------|----------|
| W   | 1   | VMH<br>7 | VMH<br>6 | VMH<br>5 | VMH<br>4 | VMH<br>3 | VMH<br>2 | VMH<br>1 | VMH<br>0 |
| R   | 1   | VMH<br>7 | VMH<br>6 | VMH<br>5 | VMH<br>4 | VMH<br>3 | VMH<br>2 | VMH<br>1 | VMH<br>0 |

Figure 6.36: Vcom control 2 register (PAGE0 -24h)

| R/W | DNC | RB7      | RB6      | RB5      | RB4      | RB3      | RB2      | RB1      | RB0      |
|-----|-----|----------|----------|----------|----------|----------|----------|----------|----------|
| W   | 1   | VML<br>7 | VML<br>6 | VML<br>5 | VML<br>4 | VML<br>3 | VML<br>2 | VML<br>1 | VML<br>0 |
| R   | 1   | VML<br>7 | VML<br>6 | VML<br>5 | VML<br>4 | VML<br>3 | VML<br>2 | VML<br>1 | VML<br>0 |

Figure 6.37: Vcom control 3 register (PAGE0 -25h)

This command is used to set VCOM Voltage include VCOM Low and VCOM High Voltage

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**VMH[7:0]:** Set the VCOMH voltage (High level voltage of VCOM). VCOM High voltage = Decimal(VMH[7:0])x0.015+2.5.

| VMH7 | VMH6 | VMH5 | VMH4 | VMH3 | VMH2 | VMH1 | VMH0 | VCOMH<br>(DDVDH_TRI=0) | VCOMH<br>(DDVDH_TRI=1) |
|------|------|------|------|------|------|------|------|------------------------|------------------------|
| 0    | 0    | 0    | 0    | 0    | 0    | 0    | 0    | 2.500                  | 2.500                  |
| 0    | 0    | 0    | 0    | 0    | 0    | 0    | 1    | 2.515                  | 2.515                  |
| 0    | 0    | 0    | 0    | 0    | 0    | 1    | 0    | 2.530                  | 2.530                  |
| 0    | 0    | 0    | 0    | 0    | 0    | 1    | 1    | 2.545                  | 2.545                  |
| 0    | 0    | 0    | 0    | 0    | 1    | 0    | 0    | 2.560                  | 2.560                  |
| 0    | 0    | 0    | 0    | 0    | 1    | 0    | 1    | 2.575                  | 2.575                  |
| :    | :    | :    | :    | :    | :    | :    | :    | :                      | :                      |
| :    | :    | :    | :    | :    | :    | :    | :    | :                      | :                      |
| 1    | 0    | 0    | 1    | 0    | 0    | 1    | 1    | 4.705                  | 4.705                  |
| 1    | 0    | 0    | 1    | 0    | 1    | 0    | 0    | 4.720                  | 4.720                  |
| 1    | 0    | 0    | 1    | 0    | 1    | 0    | 1    | 4.735                  | 4.735                  |
| 1    | 0    | 0    | 1    | 0    | 1    | 1    | 0    | 4.750                  | 4.750                  |
| 1    | 0    | 0    | 1    | 0    | 1    | 1    | 1    | 4.765                  | 4.765                  |
| 1    | 0    | 0    | 1    | 1    | 0    | 0    | 0    | 4.780                  | 4.780                  |
| 1    | 0    | 0    | 1    | 1    | 0    | 0    | 1    | 4.795                  | 4.795                  |
| 1    | 0    | 0    | 1    | 1    | 0    | 1    | 0    | 4.800                  | 4.810                  |
| 1    | 0    | 0    | 1    | 1    | 0    | 1    | 1    | 4.800                  | 4.825                  |
| 1    | 0    | 0    | 1    | 1    | 1    | 0    | 0    | 4.800                  | 4.840                  |
| 1    | 0    | 0    | 1    | 1    | 1    | 0    | 1    | 4.800                  | 4.855                  |
| :    | :    | :    | :    | :    | :    | :    | :    | 4.800                  | :                      |
| 1    | 1    | 0    | 0    | 1    | 0    | 0    | 0    | 4.800                  | 5.800                  |
| :    | :    | :    | :    | :    | :    | :    | :    | 4.800                  | 5.800                  |
| 1    | 1    | 1    | 1    | 1    | 1    | 1    | 0    | 4.800                  | 5.800                  |
| 1    | 1    | 1    | 1    | 1    | 1    | 1    | 1    | Setting inhibited      |                        |

**Note:** Internal VREF can be modified by customer's request. default VREF=4.8 if DDVDH\_TRI=0, and VREF=5.8 if DDVDH\_TRI=1

**VCOMH**= { Decimal(VMH[7:0])x0.015+2.5 }\*(VREF/4.8) if DDVDH\_TRI=0

**VCOMH**= { Decimal(VMH[7:0])x0.015+2.5 }\*(VREF/5.8) if DDVDH\_TRI=1

**VML[7:0]:** Set the VCOML voltage (Low level voltage of VCOM). VCOM Low voltage = Decimal(VML[7:0])x0.015-2.5.

| VML7 | VML6 | VML5 | VML4 | VML3 | VML2 | VML1 | VML0 | VCOML  |
|------|------|------|------|------|------|------|------|--------|
| 0    | 0    | 0    | 0    | 0    | 0    | 0    | 0    | -2.500 |
| 0    | 0    | 0    | 0    | 0    | 0    | 0    | 1    | -2.485 |
| 0    | 0    | 0    | 0    | 0    | 0    | 1    | 0    | -2.470 |
| 0    | 0    | 0    | 0    | 0    | 1    | 0    | 1    | -2.455 |
| :    | :    | :    | :    | :    | :    | :    | :    | :      |
| 1    | 0    | 1    | 0    | 0    | 0    | 1    | 1    | -0.055 |
| 1    | 0    | 1    | 0    | 0    | 1    | 0    | 0    | -0.040 |
| 1    | 0    | 1    | 0    | 0    | 1    | 0    | 1    | -0.025 |
| 1    | 0    | 1    | 0    | 0    | 1    | 1    | 0    | -0.010 |
| 1    | 0    | 1    | 0    | 0    | 1    | 1    | 1    | VSS    |
| :    | :    | :    | :    | :    | :    | :    | :    | :      |
| 1    | 1    | 1    | 1    | 1    | 1    | 1    | 1    | VSS    |

**Note:** Internal VREF can be modified by customer's request. default VREF=4.8 if DDVDH\_TRI=0 and VREF=5.8 if DDVDH\_TRI=1

**VCOML**= { Decimal ( VML[7:0])x0.015-2.5 }\*(VREF/4.8) if DDVDH\_TRI=0,

**VCOML**= { Decimal ( VML[7:0])x0.015-2.5 }\*(VREF/5.8) if DDVDH\_TRI=1

**VMF[7:0]:** Set the VCOM offset voltage. VMH+1d/VML+1d means VMH/VML from original setting move up one step (15mV). VMH-1d/VML-1d means VMH/VML from original setting move down one step (15mV)

| VMF[7:0] | VCOMH        | VCOML        |
|----------|--------------|--------------|
| 0        | "VMH" - 128d | "VMH" - 128d |
| 1        | "VMH" - 127d | "VMH" - 127d |
| 2        | "VMH" - 126d | "VMH" - 126d |
| 3        | "VMH" - 125d | "VMH" - 125d |
| :        | :            | :            |
| 126      | "VMH" - 2d   | "VMH" - 2d   |
| 127      | "VMH" - 1d   | "VMH" - 1d   |
| 128      | "VMH"        | "VML"        |
| 129      | "VMH" + 1d   | "VMH" + 1d   |
| 130      | "VMH" + 2d   | "VMH" + 2d   |
| :        | :            | :            |
| 254      | "VMH" + 126d | "VMH" + 126d |
| 255      | "VMH" + 127d | "VMH" + 127d |

**Note:** VMH[7:0]-128+VMF[7:0]>=0 and VML[7:0]-128+VMF[7:0]>=0

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## 6.26 Display control 1 register (PAGE0 -26h~R28h)

| RW | DNC | RB7 | RB6 | RB5 | RB4 | RB3  | RB2  | RB1  | RB0  |
|----|-----|-----|-----|-----|-----|------|------|------|------|
| W  | 1   | *   | *   | *   | *   | ISC3 | ISC2 | ISC1 | ISC0 |
| R  | 1   | *   | *   | *   | *   | ISC3 | ISC2 | ISC1 | ISC0 |

Figure 6.38: Display control 1 register (PAGE0 -26h)

| RW | DNC | RB7 | RB6 | RB5   | RB4   | RB3 | RB2 | RB1 | RB0 |
|----|-----|-----|-----|-------|-------|-----|-----|-----|-----|
| W  | 1   | PT1 | PT0 | PTV 1 | PTV 0 | *   | *   | PTG | REF |
| R  | 1   | PT1 | PT0 | PTV 1 | PTV 0 | *   | *   | PTG | REF |

Figure 6.39: Display control 2 register (PAGE0 -27h)

| RW | DNC | RB7 | RB6 | RB5 | RB4 | RB3 | RB2 | RB1 | RB0 |
|----|-----|-----|-----|-----|-----|-----|-----|-----|-----|
| W  | 1   | *   | *   | GON | DTE | D1  | D0  | *   | *   |
| R  | 1   | *   | *   | GON | DTE | D1  | D0  | 0   | 0   |

Figure 6.40: Display control 3 register (PAGE0 -28h)

**ISC[3:0]:** Specify the scan cycle of gate driver when **REF** = '1' in non-display area. Then scan cycle is set to an odd number from 0~31. The polarity is inverted every scan cycle.

| ISC3 | ISC2 | ISC1 | ISC0 | Scan Cycle        | $f_{FLM} = 60\text{Hz}$ |
|------|------|------|------|-------------------|-------------------------|
| 0    | 0    | 0    | 0    | 1 frame           | 17ms                    |
| 0    | 0    | 0    | 1    | 5 frames          | 83ms                    |
| 0    | 0    | 1    | 0    | 9 frames          | 150ms                   |
| 0    | 0    | 1    | 1    | 13 frames         | 217ms                   |
| 0    | 1    | 0    | 0    | 17 frames         | 283ms                   |
| 0    | 1    | 0    | 1    | 21 frames         | 350ms                   |
| 0    | 1    | 1    | 0    | 25 frames         | 417ms                   |
| 0    | 1    | 1    | 1    | 29 frames         | 483ms                   |
| 1    | 0    | 0    | 0    | 33 frames         | 550ms                   |
| 1    | 0    | 0    | 1    | 37 frames         | 616ms                   |
| 1    | 0    | 1    | 0    | 41 frames         | 683ms                   |
| 1    | 0    | 1    | 1    | 45 frames         | 750ms                   |
| 1    | 1    | 0    | 0    | 49 frames         | 816ms                   |
| 1    | 1    | 0    | 1    | 53 frames         | 883ms                   |
| 1    | 1    | 1    | 0    | 57 frames         | 950ms                   |
| 1    | 1    | 1    | 1    | Setting inhibited |                         |

**REF:** Refresh display in non-display area in Partial mode enable bit.  
 REF = '0': Refresh display operation is disabling.  
 REF = '1': Refresh display operation is enabling.

**PTG:** Specify the scan mode of gate driver in non-display area.

| PTG | Gate Outputs in Non-display Area |
|-----|----------------------------------|
| 0   | Normal Drive                     |
| 1   | Fixed VGL                        |

**PTV[1:0]:** Specify the scan mode of VCOM in non-display area.

| PTV1 | PTV0 | VCOM Outputs in Non-display Area |
|------|------|----------------------------------|
| 0    | 0    | Normal Drive                     |
| 0    | 1    | Fixed to VCOML                   |
| 1    | 0    | Fixed to GND                     |
| 1    | 1    | Setting Inhibited                |

**PT[1:0] :** Specify the Non-display area source output in partial display mode.

| REV_panel                   | GRAM Data                 | Source Output Level |                  |                  |            |             |            |             |            |
|-----------------------------|---------------------------|---------------------|------------------|------------------|------------|-------------|------------|-------------|------------|
|                             |                           | Display area        |                  | Non-display Area |            |             |            |             |            |
|                             |                           | VCOM = "L"          | VCOM = "H"       | PT1-0=(0,*)      |            | PT1-0=(1,0) |            | PT1-0=(1,1) |            |
|                             |                           |                     |                  | VCOM = "L"       | VCOM = "H" | VCOM = "L"  | VCOM = "H" | VCOM = "L"  | VCOM = "H" |
| 1<br>(Normally Black Panel) | 18'h0000<br>:<br>18'h3FFF | V63P<br>:<br>V0P    | V0N<br>:<br>V63N | V63P             | V0N        | VSSD        | VSSD       | Hi-z        | Hi-z       |
| 0<br>(Normally White Panel) | 18'h0000<br>:<br>18'h3FFF | V0P<br>:<br>V63P    | V63N<br>:<br>V0N | V63P             | V0N        | VSSD        | VSSD       | Hi-z        | Hi-z       |

**D[1:0]:** When D1='1', display is on; when D1='0', display is off. When display is off, the display data is retained in the GRAM, and can be instantly displayed by setting D1 = '1'. When D1='0', the display is off with the entire source outputs are set to the VSSD level. Because of this, the HX8347-G can control the charging current for the LCD with AC driving. Control the display on/off while control GON and DTE.

When D[1:0]= '01', the internal display of the HX8347-G is performed although the actual display is off. When D[1:0]= '00', the internal display operation halts and the display is off.

| D1 | D0 | Source Output | HX8347-G Internal Display Operations | Gate-Driver Control Signals |
|----|----|---------------|--------------------------------------|-----------------------------|
| 0  | 0  | VSSD          | Halt                                 | Halt                        |
| 0  | 1  | VSSD          | Operate                              | Operate                     |
| 1  | 0  | =PT(0,0)      | Operate                              | Operate                     |
| 1  | 1  | Display       | Operate                              | Operate                     |

**GON, DTE:**

| GON | DTE | Gate Output |
|-----|-----|-------------|
| 0   | X   | VGH         |
| 1   | 0   | VGL         |
| 1   | 1   | VGH/VGL     |

| PT1 | PT0 | REF | ISC[3:0]                               | Source Output  | VCOM Output                    | Gate Output               |
|-----|-----|-----|--|--|--------------------------------|---------------------------|
| 0   | x   | x   | -                                      | Black Display<br>(REV_PANEL = '1')<br>White Display<br>(REV_PANEL = '0')             | Normal Driving                 | Normal Driving            |
| 1   | 0   | 0   | -                                      | GND  | PTV[1:0]                       | PTG                       |
|     |     | 1   | Non-refresh cycle<br><br>Refresh cycle | GND<br><br>Black Display<br>(REV_PANEL = '1')<br>White Display<br>(REV_PANEL = '0')  | PTV[1:0]<br><br>Normal Driving | PTG<br><br>Normal Driving |
| 1   | 1   | 0   | -                                      | Hi-z   | PTV[1:0]                       | PTG                       |
|     |     | 1   | Non-refresh cycle<br><br>Refresh cycle | Hi-z<br><br>Black Display<br>(REV_PANEL = '1')<br>White Display<br>(REV_PANEL = '0') | PTV[1:0]<br><br>Normal Driving | PTG<br><br>Normal Driving |

6.27 Frame control register (PAGE0 -29h~R2Ch)

|           |            |           |           |           |           |          |          |          |          |
|-----------|------------|-----------|-----------|-----------|-----------|----------|----------|----------|----------|
| <b>RW</b> | <b>DNC</b> | RB7       | RB6       | RB5       | RB4       | RB3      | RB2      | RB1      | RB0      |
| <b>W</b>  | <b>1</b>   | I/P_R TN3 | I/P_R TN2 | I/P_R TN1 | I/P_R TN0 | N/P_RTN3 | N/P_RTN2 | N/P_RTN1 | N/P_RTN0 |
| <b>R</b>  | <b>1</b>   | I/P_R TN3 | I/P_R TN2 | I/P_R TN1 | I/P_R TN0 | N/P_RTN3 | N/P_RTN2 | N/P_RTN1 | N/P_RTN0 |

Figure 6.41: Frame control 1 register (PAGE0 -29h)

|           |            |     |     |          |          |     |     |          |          |
|-----------|------------|-----|-----|----------|----------|-----|-----|----------|----------|
| <b>RW</b> | <b>DNC</b> | RB7 | RB6 | RB5      | RB4      | RB3 | RB2 | RB1      | RB0      |
| <b>W</b>  | <b>1</b>   | *   | *   | I/P_DIV1 | I/P_DIV0 | *   | *   | N/P_DIV1 | N/P_DIV0 |
| <b>R</b>  | <b>1</b>   | *   | *   | I/P_DIV1 | I/P_DIV0 | *   | *   | N/P_DIV1 | N/P_DIV0 |

Figure 6.42: Frame control 2 register (PAGE0 -2Ah)

|           |            |           |           |           |           |           |           |           |           |
|-----------|------------|-----------|-----------|-----------|-----------|-----------|-----------|-----------|-----------|
| <b>RW</b> | <b>DNC</b> | RB7       | RB6       | RB5       | RB4       | RB3       | RB2       | RB1       | RB0       |
| <b>W</b>  | <b>1</b>   | N/P_DUM 7 | N/P_DUM 6 | N/P_DUM 5 | N/P_DUM 4 | N/P_DUM 3 | N/P_DUM 2 | N/P_DUM 1 | N/P_DUM 0 |
| <b>R</b>  | <b>1</b>   | N/P_DUM 7 | N/P_DUM 6 | N/P_DUM 5 | N/P_DUM 4 | N/P_DUM 3 | N/P_DUM 2 | N/P_DUM 1 | N/P_DUM 0 |

Figure 6.43: Frame control 3 register (PAGE0 -2Bh)

|           |            |            |            |            |            |            |            |            |            |
|-----------|------------|------------|------------|------------|------------|------------|------------|------------|------------|
| <b>RW</b> | <b>DNC</b> | RB7        | RB6        | RB5        | RB4        | RB3        | RB2        | RB1        | RB0        |
| <b>W</b>  | <b>1</b>   | I/PI_DUM 7 | I/PI_DUM 6 | I/PI_DUM 5 | I/PI_DUM 4 | I/PI_DUM 3 | I/PI_DUM 2 | I/PI_DUM 1 | I/PI_DUM 0 |
| <b>R</b>  | <b>1</b>   | I/PI_DUM 7 | I/PI_DUM 6 | I/PI_DUM 5 | I/PI_DUM 4 | I/PI_DUM 3 | I/PI_DUM 2 | I/PI_DUM 1 | I/PI_DUM 0 |

Figure 6.44: Frame control 4 register (PAGE0 -2Ch)

**N/P\_DIV[1:0]:** Specify the division ratio of internal clocks in Normal / Partial mode for internal operation. When used internal clock for the display operation, frame frequency can be adjusted with the **N/P\_RTN[3:0]** bits (1H period clock cycle), **N/P\_DIV[1:0]**, and **N/P\_DUM[7:0]** bits.

**I/PI\_DIV[1:0]:** Specify the division ratio of internal clocks in Idle (8-color) / Partial Idle mode for internal operation. When used internal clock for the display operation, frame frequency can be adjusted with the **I/PI\_RTN[3:0]** bits(1H period clock cycle), **I/PI\_DIV[1:0]**, and **I/PI\_DUM[7:0]** bits.

| DIV1 | DIV0 | Division Ratio | Internal Display Operation Clock Frequency |
|------|------|----------------|--|
| 0    | 0    | 1              | fosc / 1                                   |
| 0    | 1    | 2              | fosc / 2                                   |
| 1    | 0    | 4              | fosc / 4                                   |
| 1    | 1    | 8              | fosc / 8                                   |

Note: fosc = R-C oscillation frequency



**N/P\_RTN[3:0]:** Specify clock number of one line period in Normal / Partial mode for internal operation.

**I/PI\_RTN[3:0]:** Specify clock number of one line period in Idle (8-color) / Partial Idle mode for internal operation.

Clock cycles=1/internal operation clock frequency(fosc)

| RTN[3:0] | Clock number per Line | RTN[3:0] | Clock number per Line |
|----------|-----------------------|----------|-----------------------|
| 4'b0000  | 124                   | 4'b1000  | 132                   |
| 4'b0001  | 125                   | 4'b1001  | 133                   |
| 4'b0010  | 126                   | 4'b1010  | 134                   |
| 4'b0011  | 127                   | 4'b1011  | 135                   |
| 4'b0100  | 128                   | 4'b1100  | 136                   |
| 4'b0101  | 129                   | 4'b1101  | 137                   |
| 4'b0110  | 130                   | 4'b1110  | 138                   |
| 4'b0111  | 131                   | 4'b1111  | 139                   |

**N/P\_DUM[7:0]:** Specify dummy line number in blanking area of one frame in Normal / Partial mode for internal operation.

**I/PI\_DUM[7:0]:** Specify dummy line number in blanking area of one frame in Idle (8-color) / Partial Idle mode for internal operation.

| DUM[7:0] | Line Number in Blanking Period |
|----------|--------------------------------|
| 000d     | Setting Inhibited              |
| 001d     | Setting Inhibited              |
| 002d     | 2                              |
| 003d     | 3                              |
| 004d     | 4                              |
| :        | :                              |
| 190d     | 190                            |
| others   | Setting Inhibited              |

**Formula for the Frame Frequency during internal display mode:**

$$\text{Frame frequency} = \text{fosc} / (\text{RTN} \times \text{DIV} \times (320 + \text{DUM})) \text{ [Hz]}$$

fosc: RC oscillation frequency

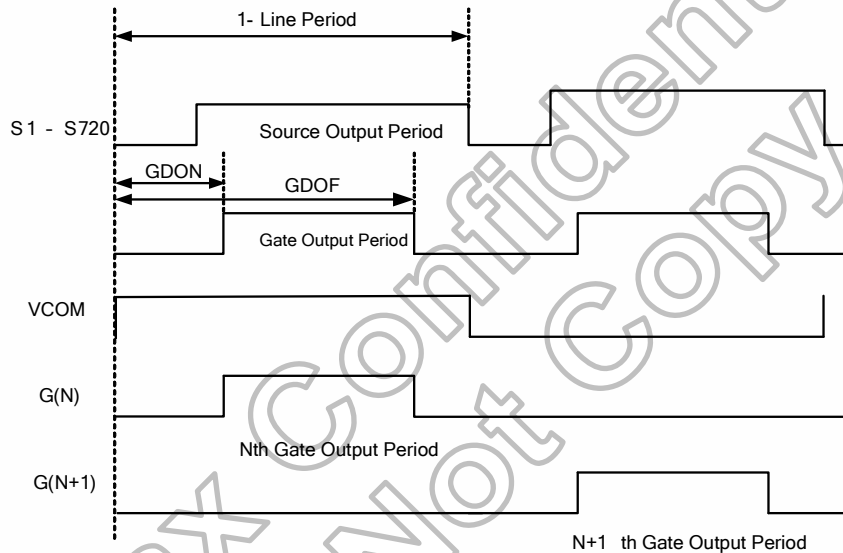
6.28 Cycle control register (PAGE0 -2Dh~R2Eh)

| R/W | DNC | RB7    | RB6    | RB5    | RB4    | RB3    | RB2    | RB1    | RB0    |
|-----|-----|--------|--------|--------|--------|--------|--------|--------|--------|
| W   | 1   | GDO N7 | GDO N6 | GDO N5 | GDO N4 | GDO N3 | GDO N2 | GDO N1 | GDO N0 |
| R   | 1   | GDO N7 | GDO N6 | GDO N5 | GDO N4 | GDO N3 | GDO N2 | GDO N1 | GDO N0 |

Figure 6.45: Cycle control register 1 (PAGE0 -2Dh)

| R/W | DNC | RB7    | RB6    | RB5    | RB4    | RB3    | RB2    | RB1    | RB0    |
|-----|-----|--------|--------|--------|--------|--------|--------|--------|--------|
| W   | 1   | GDO F7 | GDO F6 | GDO F5 | GDO F4 | GDO F3 | GDO F2 | GDO F1 | GDO F0 |
| R   | 1   | GDO F7 | GDO F6 | GDO F5 | GDO F4 | GDO F3 | GDO F2 | GDO F1 | GDO F0 |

Figure 6.46: Cycle control register 2 (PAGE0 -2Eh)



**GDON[7:0]:** Specify the valid gate output start time in 1-line driving period. The period time value is defined as SYSCLK number in internal clock display mode. The period time value is defined as DOTCLK number in 18/16-bit bus width RGB display mode and is defined as DOTCLK/3 number in 6-bit bus width RGB display mode. (Please note that the setting “00h”, “01h”, “02h” is inhibited).

**GDOF[7:0]:** Specify the gate output end time in 1-line driving period. The period time value is defined as SYSCLK number in internal clock display mode. The period time value is defined as DOTCLK number in 18/16-bit bus width RGB display mode and is defined as DOTCLK/3 number in 6-bit bus width RGB display mode.

(Please note that the  $GDON[7:0] + 1 \leq GDOF[7:0] \leq RTN-1$ ).

**6.29 Display inversion register (PAGE0 -2Fh)**

|            |            |     |              |              |              |     |             |             |             |
|------------|------------|-----|--------------|--------------|--------------|-----|-------------|-------------|-------------|
| <b>R/W</b> | <b>DNC</b> | RB7 | RB6          | RB5          | RB4          | RB3 | RB2         | RB1         | RB0         |
| W          | 1          | *   | I/PI_<br>NW2 | I/PI_<br>NW1 | I/PI_<br>NW0 | *   | N/P_<br>NW2 | N/P_<br>NW1 | N/P_<br>NW0 |
| R          | 1          | *   | I/PI_<br>NW2 | I/PI_<br>NW1 | I/PI_<br>NW0 | *   | N/P_<br>NW2 | N/P_<br>NW1 | N/P_<br>NW0 |

**Figure 6.47: Cycle control register (PAGE0 -2Fh)**

**N/P\_ NW[2:0]:** Specify LCD driving inversion type in Normal/ Partial mode.

**I/PI\_ NW[2:0]:** Specify LCD driving inversion type in Idle / Partial Idle mode.

| NW[2:0] | LCD Driving Inversion Type |
|---------|----------------------------|
| 0d      | Frame inversion            |
| 1d      | 1-line inversion           |
| 2d      | 2-line inversion           |
| 3d      | 3-line inversion           |
| :       | :                          |
| 6d      | 6-line inversion           |
| 7d      | 7-line inversion           |

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**6.30 RGB interface control register (PAGE0 -31h~R34h)**

| RW | DNC | RB7 | RB6 | RB5 | RB4 | RB3 | RB2 | RB1      | RB0      |
|----|-----|-----|-----|-----|-----|-----|-----|----------|----------|
| W  | 1   | *   | *   | *   | *   | *   | *   | RCM<br>1 | RCM<br>0 |
| R  | 1   | 0   | 0   | 0   | 0   | 0   | 0   | RCM<br>1 | RCM<br>0 |

Figure 6.48: RGB interface control register (PAGE0 -31h)

| RW | DNC | RB7 | RB6 | RB5 | RB4 | RB3 | RB2  | RB1  | RB0 |
|----|-----|-----|-----|-----|-----|-----|------|------|-----|
| W  | 1   | *   | *   | *   | *   | DPL | HSPL | VSPL | EPL |
| R  | 1   | 0   | 0   | 0   | *   | DPL | HSPL | VSPL | EPL |

Figure 6.49: RGB interface control register (PAGE0 -32h)

| RW | DNC | RB7  | RB6  | RB5  | RB4  | RB3  | RB2  | RB1  | RB0  |
|----|-----|------|------|------|------|------|------|------|------|
| W  | 1   | HBP7 | HBP6 | HBP5 | HBP4 | HBP3 | HBP2 | HBP1 | HBP0 |
| R  | 1   | HBP7 | HBP6 | HBP5 | HBP4 | HBP3 | HBP2 | HBP1 | HBP0 |

Figure 6.50: RGB interface control register (PAGE0 -33h)

| RW | DNC | RB7  | RB6  | RB5  | RB4  | RB3  | RB2  | RB1  | RB0  |
|----|-----|------|------|------|------|------|------|------|------|
| W  | 1   | HBP9 | HBP8 | VBP5 | VBP4 | VBP3 | VBP2 | VBP1 | VBP0 |
| R  | 1   | HBP9 | HBP8 | VBP5 | VBP4 | VBP3 | VBP2 | VBP1 | VBP0 |

Figure 6.51: RGB interface control register (PAGE0 -34h)

This command is used to set RGB interface related register

**RCM[1:0]:** RGB and MCU interface select.

| RCM1 | RCM0 | Interface Select                |
|------|------|---------------------------------|
| 0    | x    | System Interface <sup>(1)</sup> |
| 1    | 0    | RGB Interface(1) (VS+HS+DE)     |
| 1    | 1    | RGB Interface(2) (VS+HS)        |

Note: (1) As RCM[1:0] bit be written, the external pin RCM[1:0] control is invalid.

**EPL:** Specify the polarity of ENABLE signal in RGB interface mode. EPL='1', the ENABLE signal is High active; EPL=0, the ENABLE signal is Low active.

| EPL | ENABLE pin | Display image | Operation           |
|-----|------------|---------------|---------------------|
| 0   | High       | Enable        | Write data to D17-0 |
| 0   | Low        | Disable       | Disable             |
| 1   | High       | Disable       | Disable             |
| 1   | Low        | Enable        | Write data to D17-0 |

**VSPL:** The polarity of VSYNC pin. When VSPL='0', the VSYNC signal is Low active. When VSPL=1, the VSYNC signal is High active.

**HSPL:** The polarity of HSYNC pin. When HSPL='0', the HSYNC signal is Low active. When HSPL=1, the HSYNC signal is High active.

**DPL:** The polarity of DOTCLK pin. When DPL='0', the data is latched by the chip on the rising edge of DOTCLK signal. When DPL='1', the data is latched by the chip on the falling edge of DOTCLK signal.

**HBP** and **VBP** are used to set vertical and horizontal back porch control in RGB I/F mode 2 (RCM[1:0]='11') (RGB I/F mode 1 is using DE signal as data enable signal)

**HBP[9:0]:** Set the delay period from falling edge of HSYNC signal to first valid data in RGB I/F mode 2

| HBP[9:0] | No. of Clock Cycle of DOTCLK |
|----------|------------------------------|
| 00d      | Setting Inhibited            |
| 01d      | Setting Inhibited            |
| 02d      | 2                            |
| 03d      | 3                            |
| 04d      | 4                            |
| :        | :                            |
| 1021d    | 1021                         |
| 1022d    | 1022                         |
| 1023d    | Setting Inhibited            |

**VBP[5:0]:** Set the delay period from falling edge of VSYNC signal to first valid line in RGB I/F mode 2

| VBP[5:0] | No. of Clock Cycle of HSYNC |
|----------|-----------------------------|
| 00d      | Setting Inhibited           |
| 01d      | Setting Inhibited           |
| 02d      | 2                           |
| 03d      | 3                           |
| 04d      | 4                           |
| :        | :                           |
| 125d     | 125                         |
| 126d     | 126                         |
| 127d     | Setting Inhibited           |

**6.31 Panel characteristic control register (PAGE0 -36h)**

| R/W | DNC | RB7 | RB6 | RB5 | RB4 | RB3          | RB2          | RB1           | RB0           |
|-----|-----|-----|-----|-----|-----|--------------|--------------|---------------|---------------|
| W   | 1   | *   | *   | *   | *   | SS_PA<br>NEL | GS_PA<br>NEL | REV_P<br>ANEL | BGR_P<br>ANEL |
| R   | 1   | *   | *   | *   | *   | SS_PA<br>NEL | GS_PA<br>NEL | REV_P<br>ANEL | BGR_P<br>ANEL |

**Figure 6.52: Panel characteristic control register (PAGE0 -36h)**

This command is internal use for display panel setting.

**REV\_PANEL:** The source output data polarity selected.

'0': normally white panel.

'1': normally black panel.

**BGR\_PANEL:** The color filter order direction selected.

'0': S1:S2:S3='R':'G':'B'

'1': S1:S2:S3='B':'G':'R'

**GS\_PANEL:** The gate driver output shift direction selected.

'0': G1→G320

'1': G320→G1

**SS\_PANEL:** The source driver output shift direction selected.

'0': S720→S1

'1': S1→S720

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**6.32 OTP register (PAGE0 -38h ~ R3Ah)**

| R/W | DNC | D7           | D6           | D5             | D4             | D3          | D2            | D1            | D0          |
|-----|-----|--------------|--------------|----------------|----------------|-------------|---------------|---------------|-------------|
| W   | 1   | OTP_PT<br>M1 | OTP_PT<br>M0 | OTP_VR<br>ADJ1 | OTP_VR<br>ADJ0 | OTP_PO<br>R | OTP_OT<br>PEN | OTP_PP<br>ROG | OTP_PW<br>E |
| R   | 1   | OTP_PT<br>M1 | OTP_PT<br>M0 | OTP_VR<br>ADJ1 | OTP_VR<br>ADJ0 | OTP_PO<br>R | OTP_OT<br>PEN | OTP_PP<br>ROG | OTP_PW<br>E |

**Figure 6.53: OTP command 1 (PAGE0 -38h)**

| R/W | RS | D7 | D6 | D5 | D4 | D3 | D2      | D1      | D0      |
|-----|----|----|----|----|----|----|---------|---------|---------|
| W   | 1  | *  | *  | *  | *  | *  | OTP_YA2 | OTP_YA1 | OTP_YA0 |
| R   | 1  | *  | *  | *  | *  | *  | OTP_YA2 | OTP_YA1 | OTP_YA0 |

**Figure 6.54: OTP command 2 (PAGE0 -39h)**

| R/W | RS | D7 | D6 | D5 | D4      | D3      | D2      | D1      | D0      |
|-----|----|----|----|----|---------|---------|---------|---------|---------|
| W   | 1  | *  | *  | *  | OTP_XA4 | OTP_XA3 | OTP_XA2 | OTP_XA1 | OTP_XA0 |
| R   | 1  | *  | *  | *  | OTP_XA4 | OTP_XA3 | OTP_XA2 | OTP_XA1 | OTP_XA1 |

**Figure 6.55: OTP command 3 (PAGE0 -3Ah)**

| R/W | RS | D7            | D6            | D5            | D4            | D3            | D2            | D1            | D0            |
|-----|----|---------------|---------------|---------------|---------------|---------------|---------------|---------------|---------------|
| R   | 1  | OTP_DAT<br>A7 | OTP_DAT<br>A6 | OTP_DAT<br>A5 | OTP_DAT<br>A4 | OTP_DAT<br>A3 | OTP_DAT<br>A2 | OTP_DAT<br>A1 | OTP_DAT<br>A0 |

**Figure 6.56: OTP command 3 (PAGE0 -3Bh)**

This command is used to set the OTP related setting. Please see OTP flow for detailed use.

**OTP\_POR:** for OTP read/write timing control

**OTP\_OTPEN:** 1'b1 to select 6.5V for OTP write operation.

**OTP\_PPROG:** 1'b1 to turn on OTP write mode.

**OTP\_PWE:** 1'b1 to write OTP.

**OTP\_XA[4:0]; OTP\_YA[2:0]:** Select OTP writes address

**OTPDATA[7:0];** Read OTP data. When user want read OTP data, must set OTP index first and then set OTP\_POR=1. After this user can get OTP data from OTPDATA[7:0]

**OTP\_TM[1:0]:** OTP Test mode register, In-house use.

**OTP\_VRADJ[1:0]:** OTP VPP2 adjusts register, In-house use.



**6.33 CABC control 1~4 register (PAGE0 -3Ch~3Fh)**

| R/W | DNC | RB7      | RB6      | RB5      | RB4      | RB3      | RB2      | RB1      | RB0      |
|-----|-----|----------|----------|----------|----------|----------|----------|----------|----------|
| W   | 1   | DBV<br>7 | DBV<br>6 | DBV<br>5 | DBV<br>4 | DBV<br>3 | DBV<br>2 | DBV<br>1 | DBV<br>0 |
| R   | 1   | DBV<br>7 | DBV<br>6 | DBV<br>5 | DBV<br>4 | DBV<br>3 | DBV<br>2 | DBV<br>1 | DBV<br>0 |

Figure 6.57: CABC control 1 register (PAGE0 -3Ch)

| R/W | DNC | RB7 | RB6 | RB5       | RB4 | RB3 | RB2 | RB1 | RB0 |
|-----|-----|-----|-----|-----------|-----|-----|-----|-----|-----|
| W   | 1   | *   | *   | BCT<br>RL | *   | DD  | BL  | *   | *   |
| R   | 1   | 0   | 0   | BCT<br>RL | 0   | DD  | BL  | 0   | 0   |

Figure 6.58: CABC control 2 register (PAGE0 -3Dh)

| R/W | DNC | RB7 | RB6 | RB5 | RB4 | RB3 | RB2 | RB1 | RB0 |
|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|
| W   | 1   | *   | *   | *   | *   | *   | *   | C1  | C0  |
| R   | 1   | 0   | 0   | 0   | 0   | 0   | 0   | C1  | C0  |

Figure 6.59: CABC control 3 register (PAGE0 -3Eh)

| R/W | DNC | RB7      | RB6      | RB5      | RB4      | RB3      | RB2      | RB1      | RB0      |
|-----|-----|----------|----------|----------|----------|----------|----------|----------|----------|
| W   | 1   | CMB<br>7 | CMB<br>6 | CMB<br>5 | CMB<br>4 | CMB<br>3 | CMB<br>2 | CMB<br>1 | CMB<br>0 |
| R   | 1   | CMB<br>7 | CMB<br>6 | CMB<br>5 | CMB<br>4 | CMB<br>3 | CMB<br>2 | CMB<br>1 | CMB<br>0 |

Figure 6.60: CABC control 4 register (PAGE0 -3Fh)

These commands are used to set CABC parameter

**DBV[7:0]:** The backlight PWM pulse output duty is equal to  $DBV[7:0]/255 \times CABC\_duty$ .

**BCTRL:** Backlight Control Block On/Off, This bit is always used to switch brightness for display.

'0' = Off (Equal to  $DBV[7:0] = '00h'$ )

'1' = On (Brightness registers are active.)

**DD:** Display Dimming (Only for manual brightness setting)

'0': Display Dimming is off.

'1': Display Dimming is on.

**BL:** Backlight Control On/Off

'0' = Off (Completely turn off backlight circuit. Control lines must be low. )

'1' = On

Dimming function is adapted to the brightness registers for display when bit BCTRL is changed at DD=1, e.g. BCTRL: 0 -> 1 or 1-> 0.

When BL bit change from "On" to "Off", backlight is turned off without gradual dimming, even if dimming-on (DD=1) are selected.

**C[1:0]:** This command is used to set parameters for image content based adaptive brightness control functionality.

There is possible to use 4 different modes for content adaptive image functionality, which are defined on a table below.

| C1 | C0 | Function             | Note |
|----|----|----------------------|------|
| 0  | 0  | Off                  | -    |
| 0  | 1  | User Interface Image | -    |
| 1  | 0  | Still Picture        | -    |
| 1  | 1  | Moving Image         | -    |

**CMB[7:0]:** This command is used to set the minimum brightness value of the display for CABC function.

In principle relationship is that 00h value means the lowest brightness for CABC and FFh value means the highest brightness for CABC.

**6.34 Gamma control 1~35 register (PAGE0 -40h~5Dh)**

| R/W | DNC | RB7 | RB6 | RB5       | RB4       | RB3       | RB2       | RB1       | RB0       |
|-----|-----|-----|-----|-----------|-----------|-----------|-----------|-----------|-----------|
| W   | 1   | *   | *   | VRP<br>05 | VRP<br>04 | VRP<br>03 | VRP<br>02 | VRP<br>01 | VRP<br>00 |
| R   | 1   | 0   | 0   | VRP<br>05 | VRP<br>04 | VRP<br>03 | VRP<br>02 | VRP<br>01 | VRP<br>00 |

Figure 6.61: Gamma control 1 register (PAGE0 -40h)

| R/W | DNC | RB7 | RB6 | RB5       | RB4       | RB3       | RB2       | RB1       | RB0       |
|-----|-----|-----|-----|-----------|-----------|-----------|-----------|-----------|-----------|
| W   | 1   | *   | *   | VRP<br>15 | VRP<br>14 | VRP<br>13 | VRP<br>12 | VRP<br>11 | VRP<br>10 |
| R   | 1   | 0   | 0   | VRP<br>15 | VRP<br>14 | VRP<br>13 | VRP<br>12 | VRP<br>11 | VRP<br>10 |

Figure 6.62: Gamma control 2 register (PAGE0 -41h)

| R/W | DNC | RB7 | RB6 | RB5       | RB4       | RB3       | RB2       | RB1       | RB0       |
|-----|-----|-----|-----|-----------|-----------|-----------|-----------|-----------|-----------|
| W   | 1   | *   | *   | VRP<br>25 | VRP<br>24 | VRP<br>23 | VRP<br>22 | VRP<br>21 | VRP<br>20 |
| R   | 1   | 0   | 0   | VRP<br>25 | VRP<br>24 | VRP<br>23 | VRP<br>22 | VRP<br>21 | VRP<br>20 |

Figure 6.63: Gamma control 3 register (PAGE0 -42h)

| R/W | DNC | RB7 | RB6 | RB5       | RB4       | RB3       | RB2       | RB1       | RB0       |
|-----|-----|-----|-----|-----------|-----------|-----------|-----------|-----------|-----------|
| W   | 1   | *   | *   | VRP<br>35 | VRP<br>34 | VRP<br>33 | VRP<br>32 | VRP<br>31 | VRP<br>30 |
| R   | 1   | 0   | 0   | VRP<br>35 | VRP<br>34 | VRP<br>33 | VRP<br>32 | VRP<br>31 | VRP<br>30 |

Figure 6.64: Gamma control 4 register (PAGE0 -43h)

| R/W | DNC | RB7 | RB6 | RB5       | RB4       | RB3       | RB2       | RB1       | RB0       |
|-----|-----|-----|-----|-----------|-----------|-----------|-----------|-----------|-----------|
| W   | 1   | *   | *   | VRP<br>45 | VRP<br>44 | VRP<br>43 | VRP<br>42 | VRP<br>41 | VRP<br>40 |
| R   | 1   | 0   | 0   | VRP<br>45 | VRP<br>44 | VRP<br>43 | VRP<br>42 | VRP<br>41 | VRP<br>40 |

Figure 6.65: Gamma control 5 register (PAGE0 -44h)

| R/W | DNC | RB7 | RB6 | RB5       | RB4       | RB3       | RB2       | RB1       | RB0       |
|-----|-----|-----|-----|-----------|-----------|-----------|-----------|-----------|-----------|
| W   | 1   | *   | *   | VRP<br>55 | VRP<br>54 | VRP<br>53 | VRP<br>52 | VRP<br>51 | VRP<br>50 |
| R   | 1   | 0   | 0   | VRP<br>55 | VRP<br>54 | VRP<br>53 | VRP<br>52 | VRP<br>51 | VRP<br>50 |

Figure 6.66: Gamma control 6 register (PAGE0 -45h)

| R/W | DNC | RB7 | RB6       | RB5       | RB4       | RB3       | RB2       | RB1       | RB0       |
|-----|-----|-----|-----------|-----------|-----------|-----------|-----------|-----------|-----------|
| W   | 1   | *   | PRP<br>06 | PRP<br>05 | PRP<br>04 | PRP<br>03 | PRP<br>02 | PRP<br>01 | PRP<br>00 |
| R   | 1   | 0   | PRP<br>06 | PRP<br>05 | PRP<br>04 | PRP<br>03 | PRP<br>02 | PRP<br>01 | PRP<br>00 |

Figure 6.67: Gamma control 7 register (PAGE0 -46h)

| R/W | DNC | RB7 | RB6       | RB5       | RB4       | RB3       | RB2       | RB1       | RB0       |
|-----|-----|-----|-----------|-----------|-----------|-----------|-----------|-----------|-----------|
| W   | 1   | *   | PRP<br>16 | PRP<br>15 | PRP<br>14 | PRP<br>13 | PRP<br>12 | PRP<br>11 | PRP<br>10 |
| R   | 1   | 0   | PRP<br>16 | PRP<br>15 | PRP<br>14 | PRP<br>13 | PRP<br>12 | PRP<br>11 | PRP<br>10 |

Figure 6.68: Gamma control 8 register (PAGE0 -47h)

| R/W | DNC | RB7 | RB6 | RB5 | RB4       | RB3       | RB2       | RB1       | RB0       |
|-----|-----|-----|-----|-----|-----------|-----------|-----------|-----------|-----------|
| W   | 1   | *   | *   | *   | PKP<br>04 | PKP<br>03 | PKP<br>02 | PKP<br>01 | PKP<br>00 |
| R   | 1   | 0   | 0   | 0   | PKP<br>04 | PKP<br>03 | PKP<br>02 | PKP<br>01 | PKP<br>00 |

Figure 6.69: Gamma control 9 register (PAGE0 -48h)

| R/W | DNC | RB7 | RB6 | RB5 | RB4       | RB3       | RB2       | RB1       | RB0       |
|-----|-----|-----|-----|-----|-----------|-----------|-----------|-----------|-----------|
| W   | 1   | *   | *   | *   | PKP<br>14 | PKP<br>13 | PKP<br>12 | PKP<br>11 | PKP<br>10 |
| R   | 1   | 0   | 0   | 0   | PKP<br>14 | PKP<br>13 | PKP<br>12 | PKP<br>11 | PKP<br>10 |

Figure 6.70: Gamma control 10 register (PAGE0 -49h)

| R/W | DNC | RB7 | RB6 | RB5 | RB4       | RB3       | RB2       | RB1       | RB0       |
|-----|-----|-----|-----|-----|-----------|-----------|-----------|-----------|-----------|
| W   | 1   | *   | *   | *   | PKP<br>24 | PKP<br>23 | PKP<br>22 | PKP<br>21 | PKP<br>20 |
| R   | 1   | 0   | 0   | 0   | PKP<br>24 | PKP<br>23 | PKP<br>22 | PKP<br>21 | PKP<br>20 |

Figure 6.71: Gamma control 11 register (PAGE0 -4Ah)

| R/W | DNC | RB7 | RB6 | RB5 | RB4       | RB3       | RB2       | RB1       | RB0       |
|-----|-----|-----|-----|-----|-----------|-----------|-----------|-----------|-----------|
| W   | 1   | *   | *   | *   | PKP<br>34 | PKP<br>33 | PKP<br>32 | PKP<br>31 | PKP<br>30 |
| R   | 1   | 0   | 0   | 0   | PKP<br>34 | PKP<br>33 | PKP<br>32 | PKP<br>31 | PKP<br>30 |

Figure 6.72: Gamma control 12 register (PAGE0 -4Bh)

| R/W | DNC | RB7 | RB6 | RB5 | RB4       | RB3       | RB2       | RB1       | RB0       |
|-----|-----|-----|-----|-----|-----------|-----------|-----------|-----------|-----------|
| W   | 1   | *   | *   | *   | PKP<br>44 | PKP<br>43 | PKP<br>42 | PKP<br>41 | PKP<br>40 |
| R   | 1   | 0   | 0   | 0   | PKP<br>44 | PKP<br>43 | PKP<br>42 | PKP<br>41 | PKP<br>40 |

Figure 6.73: Gamma control 13 register (PAGE0 -4Ch)

| R/W | DNC | RB7 | RB6 | RB5       | RB4       | RB3       | RB2       | RB1       | RB0       |
|-----|-----|-----|-----|-----------|-----------|-----------|-----------|-----------|-----------|
| W   | 1   | *   | *   | VRN<br>05 | VRN<br>04 | VRN<br>03 | VRN<br>02 | VRN<br>01 | VRN<br>00 |
| R   | 1   | 0   | 0   | VRN<br>05 | VRN<br>04 | VRN<br>03 | VRN<br>02 | VRN<br>01 | VRN<br>00 |

Figure 6.74: Gamma control 14 register (PAGE0 -50h)

| R/W | DNC | RB7 | RB6 | RB5       | RB4       | RB3       | RB2       | RB1       | RB0       |
|-----|-----|-----|-----|-----------|-----------|-----------|-----------|-----------|-----------|
| W   | 1   | *   | *   | VRN<br>15 | VRN<br>14 | VRN<br>13 | VRN<br>12 | VRN<br>11 | VRN<br>10 |
| R   | 1   | 0   | 0   | VRN<br>15 | VRN<br>14 | VRN<br>13 | VRN<br>12 | VRN<br>11 | VRN<br>10 |

Figure 6.75: Gamma control 15 register (PAGE0 -51h)

| R/W | DNC | RB7 | RB6 | RB5       | RB4       | RB3       | RB2       | RB1       | RB0       |
|-----|-----|-----|-----|-----------|-----------|-----------|-----------|-----------|-----------|
| W   | 1   | *   | *   | VRN<br>25 | VRN<br>24 | VRN<br>23 | VRN<br>22 | VRN<br>21 | VRN<br>20 |
| R   | 1   | 0   | 0   | VRN<br>25 | VRN<br>24 | VRN<br>23 | VRN<br>22 | VRN<br>21 | VRN<br>20 |

Figure 6.76: Gamma control 16 register (PAGE0 -52h)

| R/W | DNC | RB7 | RB6 | RB5       | RB4       | RB3       | RB2       | RB1       | RB0       |
|-----|-----|-----|-----|-----------|-----------|-----------|-----------|-----------|-----------|
| W   | 1   | *   | *   | VRN<br>35 | VRN<br>34 | VRN<br>33 | VRN<br>32 | VRN<br>31 | VRN<br>30 |
| R   | 1   | 0   | 0   | VRN<br>35 | VRN<br>34 | VRN<br>33 | VRN<br>32 | VRN<br>31 | VRN<br>30 |

Figure 6.77: Gamma control 17 register (PAGE0 -53h)

| R/W | DNC | RB7 | RB6 | RB5       | RB4       | RB3       | RB2       | RB1       | RB0       |
|-----|-----|-----|-----|-----------|-----------|-----------|-----------|-----------|-----------|
| W   | 1   | *   | *   | VRN<br>45 | VRN<br>44 | VRN<br>43 | VRN<br>42 | VRN<br>41 | VRN<br>40 |
| R   | 1   | 0   | 0   | VRN<br>45 | VRN<br>44 | VRN<br>43 | VRN<br>42 | VRN<br>41 | VRN<br>40 |

Figure 6.78: Gamma control 18 register (PAGE0 -54h)

| R/W | DNC | RB7 | RB6 | RB5       | RB4       | RB3       | RB2       | RB1       | RB0       |
|-----|-----|-----|-----|-----------|-----------|-----------|-----------|-----------|-----------|
| W   | 1   | *   | *   | VRN<br>55 | VRN<br>54 | VRN<br>53 | VRN<br>52 | VRN<br>51 | VRN<br>50 |
| R   | 1   | 0   | 0   | VRN<br>55 | VRN<br>54 | VRN<br>53 | VRN<br>52 | VRN<br>51 | VRN<br>50 |

Figure 6.79: Gamma control 19 register (PAGE0 -55h)

| R/W | DNC | RB7 | RB6       | RB5       | RB4       | RB3       | RB2       | RB1       | RB0       |
|-----|-----|-----|-----------|-----------|-----------|-----------|-----------|-----------|-----------|
| W   | 1   | *   | PRN<br>06 | PRN<br>05 | PRN<br>04 | PRN<br>03 | PRN<br>02 | PRN<br>01 | PRN<br>00 |
| R   | 1   | 0   | PRN<br>06 | PRN<br>05 | PRN<br>04 | PRN<br>03 | PRN<br>02 | PRN<br>01 | PRN<br>00 |

Figure 6.80: Gamma control 20 register (PAGE0 -56h)

| R/W | DNC | RB7 | RB6       | RB5       | RB4       | RB3       | RB2       | RB1       | RB0       |
|-----|-----|-----|-----------|-----------|-----------|-----------|-----------|-----------|-----------|
| W   | 1   | *   | PRN<br>16 | PRN<br>15 | PRN<br>14 | PRN<br>13 | PRN<br>12 | PRN<br>11 | PRN<br>10 |
| R   | 1   | 0   | PRN<br>16 | PRN<br>15 | PRN<br>14 | PRN<br>13 | PRN<br>12 | PRN<br>11 | PRN<br>10 |

Figure 6.81: Gamma control 21 register (PAGE0 -57h)

| R/W | DNC | RB7 | RB6 | RB5 | RB4       | RB3       | RB2       | RB1       | RB0       |
|-----|-----|-----|-----|-----|-----------|-----------|-----------|-----------|-----------|
| W   | 1   | *   | *   | *   | PKN<br>04 | PKN<br>03 | PKN<br>02 | PKN<br>01 | PKN<br>00 |
| R   | 1   | 0   | 0   | 0   | PKN<br>04 | PKN<br>03 | PKN<br>02 | PKN<br>01 | PKN<br>00 |

Figure 6.82: Gamma control 22 register (PAGE0 -58h)

| R/W | DNC | RB7 | RB6 | RB5 | RB4       | RB3       | RB2       | RB1       | RB0       |
|-----|-----|-----|-----|-----|-----------|-----------|-----------|-----------|-----------|
| W   | 1   | *   | *   | *   | PKN<br>14 | PKN<br>13 | PKN<br>12 | PKN<br>11 | PKN<br>10 |
| R   | 1   | 0   | 0   | 0   | PKN<br>14 | PKN<br>13 | PKN<br>12 | PKN<br>11 | PKN<br>10 |

Figure 6.83: Gamma control 23 register (PAGE0 -59h)

| R/W | DNC | RB7 | RB6 | RB5 | RB4       | RB3       | RB2       | RB1       | RB0       |
|-----|-----|-----|-----|-----|-----------|-----------|-----------|-----------|-----------|
| W   | 1   | *   | *   | *   | PKN<br>24 | PKN<br>23 | PKN<br>22 | PKN<br>21 | PKN<br>20 |
| R   | 1   | 0   | 0   | 0   | PKN<br>24 | PKN<br>23 | PKN<br>22 | PKN<br>21 | PKN<br>20 |

Figure 6.84: Gamma control 24 register (PAGE0 -5Ah)

| R/W | DNC | RB7 | RB6 | RB5 | RB4       | RB3       | RB2       | RB1       | RB0       |
|-----|-----|-----|-----|-----|-----------|-----------|-----------|-----------|-----------|
| W   | 1   | *   | *   | *   | PKN<br>34 | PKN<br>33 | PKN<br>32 | PKN<br>31 | PKN<br>30 |
| R   | 1   | 0   | 0   | 0   | PKN<br>34 | PKN<br>33 | PKN<br>32 | PKN<br>31 | PKN<br>30 |

Figure 6.85: Gamma control 25 register (PAGE0 -5Bh)

| R/W | DNC | RB7 | RB6 | RB5 | RB4       | RB3       | RB2       | RB1       | RB0       |
|-----|-----|-----|-----|-----|-----------|-----------|-----------|-----------|-----------|
| W   | 1   | *   | *   | *   | PKN<br>44 | PKN<br>43 | PKN<br>42 | PKN<br>41 | PKN<br>40 |
| R   | 1   | 0   | 0   | 0   | PKN<br>44 | PKN<br>43 | PKN<br>42 | PKN<br>41 | PKN<br>40 |

Figure 6.86: Gamma control 26 register (PAGE0 -5Ch)

| R/W | DNC | RB7        | RB6        | RB5        | RB4        | RB3        | RB2        | RB1        | RB0        |
|-----|-----|------------|------------|------------|------------|------------|------------|------------|------------|
| W   | 1   | CGM<br>N11 | CGM<br>N10 | CGM<br>N01 | CGM<br>N00 | CGM<br>P11 | CGM<br>P10 | CGM<br>P01 | CGM<br>P00 |
| R   | 1   | CGM<br>N11 | CGM<br>N10 | CGM<br>N01 | CGM<br>N00 | CGM<br>P11 | CGM<br>P10 | CGM<br>P01 | CGM<br>P00 |

Figure 6.87: Gamma control 27 register (PAGE0 -5Dh)

- VRP5-0[5:0]:** Gamma Offset adjustment registers for positive polarity output
- VRN5-0[5:0]:** Gamma Offset adjustment registers for negative polarity output
- PRP1-0[6:0]:** Gamma Center adjustment registers for positive polarity output
- PRN1-0[6:0]:** Gamma Center adjustment registers for negative polarity output
- PKP8-0[4:0]:** Gamma Macro adjustment registers for positive polarity output
- PKN8-0[4:0]:** Gamma Macro adjustment registers for negative polarity output

For details, please refer to 5.10 Gamma resister stream and 8 to 1 Selector.



**6.35 TE control register (PAGE0 -60h, 84h~85h)**

| R/W | DNC | RB7 | RB6 | RB5 | RB4     | RB3  | RB2 | RB1 | RB0 |
|-----|-----|-----|-----|-----|---------|------|-----|-----|-----|
| W   | 1   | *   | *   | *   | TEM ODE | TEON | *   | *   | *   |
| R   | 1   | 0   | 0   | 0   | TEM ODE | TEON | 0   | 0   | 0   |

Figure 6.88: TE control register (PAGE0 -60h)

| R/W | DNC | RB7     | RB6     | RB5     | RB4     | RB3     | RB2     | RB1    | RB0    |
|-----|-----|---------|---------|---------|---------|---------|---------|--------|--------|
| W   | 1   | TSE L15 | TSE L14 | TSE L13 | TSE L12 | TSE L11 | TSE L10 | TSE L9 | TSE L8 |
| R   | 1   | TSE L15 | TSE L14 | TSE L13 | TSE L12 | TSE L11 | TSE L10 | TSE L9 | TSE L8 |

Figure 6.89: TE output line2 register (PAGE0 -84h)

| R/W | DNC | RB7    | RB6    | RB5    | RB4    | RB3    | RB2    | RB1    | RB0    |
|-----|-----|--------|--------|--------|--------|--------|--------|--------|--------|
| W   | 1   | TSE L7 | TSE L6 | TSE L5 | TSE L4 | TSE L3 | TSE L2 | TSE L1 | TSE L0 |
| R   | 1   | TSE L7 | TSE L6 | TSE L5 | TSE L4 | TSE L3 | TSE L2 | TSE L1 | TSE L0 |

Figure 6.90: TE output line1 register (PAGE0 -85h)

**TEMODE:** Specify the Tearing-Effect mode.

When **TEMODE** = '0': The Tearing Effect Output line (TE) consists of V-Blanking information only.



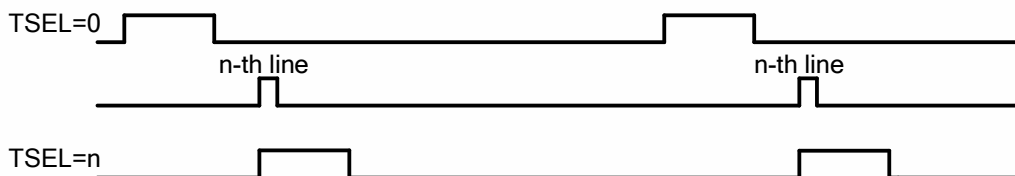
When **TEMODE** = '1': The Tearing Effect Output Line (TE) consists of both V-Blanking and H-Blanking information



**Note:** During Stand by Mode with Tearing Effect Line On, Tearing Effect Output pin active low

**TEON:** This command is used to turn ON the Tearing Effect output signal from the TE signal line.

**TSEL[15:0]:** This command is used to setting TE delay line at TEMODE="0". When TSEL[15:0]=16'h0000, TE output is the same as TEMODE="0". When Decimal(TSEL[15:0])=n, TE output at n-th line starting.



**6.36 ID register (PAGE0 -R61h~R63h)**

| R/W | DNC | RB7  | RB6  | RB5  | RB4  | RB3  | RB2  | RB1  | RB0  |
|-----|-----|------|------|------|------|------|------|------|------|
| W   | 1   | ID17 | ID16 | ID15 | ID14 | ID13 | ID12 | ID11 | ID10 |
| R   | 1   | ID17 | ID16 | ID15 | ID14 | ID13 | ID12 | ID11 | ID10 |

**Figure 6.91: ID1 register (PAGE0 -61h)**

| R/W | DNC | RB7  | RB6  | RB5  | RB4  | RB3  | RB2  | RB1  | RB0  |
|-----|-----|------|------|------|------|------|------|------|------|
| W   | 1   | ID27 | ID26 | ID25 | ID24 | ID23 | ID22 | ID21 | ID20 |
| R   | 1   | ID27 | ID26 | ID25 | ID24 | ID23 | ID22 | ID21 | ID20 |

**Figure 6.92: ID2 register (PAGE0 -62h)**

| R/W | DNC | RB7  | RB6  | RB5  | RB4  | RB3  | RB2  | RB1  | RB0  |
|-----|-----|------|------|------|------|------|------|------|------|
| W   | 1   | ID37 | ID36 | ID35 | ID34 | ID33 | ID32 | ID31 | ID30 |
| R   | 1   | ID37 | ID36 | ID35 | ID34 | ID33 | ID32 | ID31 | ID30 |

**Figure 6.93: ID3 register (PAGE0 -63h)**

**ID1~ID3:** ID setting related register.

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**6.37 Power saving internal control register (PAGE0 -RE4h~RE7h)**

| R/W | DNC | D7     | D6     | D5     | D4     | D3     | D2     | D1     | D0     |
|-----|-----|--------|--------|--------|--------|--------|--------|--------|--------|
| W   | 1   | EQ_S17 | EQ_S16 | EQ_S15 | EQ_S14 | EQ_S13 | EQ_S12 | EQ_S11 | EQ_S10 |
| R   | 1   | EQ_S17 | EQ_S16 | EQ_S15 | EQ_S14 | EQ_S13 | EQ_S12 | EQ_S11 | EQ_S10 |

**Figure 6.94: Power saving internal control register (R68h)**

| R/W | DNC | D7     | D6     | D5     | D4     | D3     | D2     | D1     | D0     |
|-----|-----|--------|--------|--------|--------|--------|--------|--------|--------|
| W   | 1   | EQ_S27 | EQ_S26 | EQ_S25 | EQ_S24 | EQ_S23 | EQ_S22 | EQ_S21 | EQ_S20 |
| R   | 1   | EQ_S27 | EQ_S26 | EQ_S25 | EQ_S24 | EQ_S23 | EQ_S22 | EQ_S21 | EQ_S20 |

**Figure 6.95: Power saving Internal control register (R69h)**

| R/W | DNC | D7     | D6     | D5     | D4     | D3     | D2     | D1     | D0     |
|-----|-----|--------|--------|--------|--------|--------|--------|--------|--------|
| W   | 1   | EQ_S37 | EQ_S36 | EQ_S35 | EQ_S34 | EQ_S33 | EQ_S32 | EQ_S31 | EQ_S30 |
| R   | 1   | EQ_S37 | EQ_S36 | EQ_S35 | EQ_S34 | EQ_S33 | EQ_S32 | EQ_S31 | EQ_S30 |

**Figure 6.96: Power saving Internal control register (R70h)**

| R/W | DNC | D7     | D6     | D5     | D4     | D3     | D2     | D1     | D0     |
|-----|-----|--------|--------|--------|--------|--------|--------|--------|--------|
| W   | 1   | EQ_S47 | EQ_S46 | EQ_S45 | EQ_S44 | EQ_S43 | EQ_S42 | EQ_S41 | EQ_S40 |
| R   | 1   | EQ_S47 | EQ_S46 | EQ_S45 | EQ_S44 | EQ_S43 | EQ_S42 | EQ_S41 | EQ_S40 |

**Figure 6.97: Power saving Internal control register (R71h)**

These commands are internal used.

**EQ\_S1[7:0]:** Power Saving control internal used.

**EQ\_S2[7:0]:** Power Saving control internal used.

**EQ\_S3[7:0]:** Power Saving control internal used.

**EQ\_S4[7:0]:** Power Saving control internal used.

**6.38 Source OP control (PAGE0 -RE8h~E9h)**

| RW       | DNC      | RB7       | RB6       | RB5       | RB4       | RB3       | RB2       | RB1       | RB0       |
|----------|----------|-----------|-----------|-----------|-----------|-----------|-----------|-----------|-----------|
| <b>W</b> | <b>1</b> | OPON_N(7) | OPON_N(6) | OPON_N(5) | OPON_N(4) | OPON_N(3) | OPON_N(2) | OPON_N(1) | OPON_N(0) |
| <b>R</b> | <b>1</b> | OPON_N(7) | OPON_N(6) | OPON_N(5) | OPON_N(4) | OPON_N(3) | OPON_N(2) | OPON_N(1) | OPON_N(0) |

**Figure 6.98: Source OP control register (PAGE0 -RE8h)**

| RW       | DNC      | RB7       | RB6       | RB5       | RB4       | RB3       | RB2       | RB1       | RB0       |
|----------|----------|-----------|-----------|-----------|-----------|-----------|-----------|-----------|-----------|
| <b>W</b> | <b>1</b> | OPON_N(7) | OPON_N(6) | OPON_N(5) | OPON_N(4) | OPON_N(3) | OPON_N(2) | OPON_N(1) | OPON_N(0) |
| <b>R</b> | <b>1</b> | OPON_N(7) | OPON_N(6) | OPON_N(5) | OPON_N(4) | OPON_N(3) | OPON_N(2) | OPON_N(1) | OPON_N(0) |

**Figure 6.99: Source OP control register (PAGE0 -RE9h)**

This command is used to set the Source OP output period. It will increase the driving ability of the source driver. For example, if the user has crosstalk issue, user can adjust this command for more driving ability, the ability is more when the setting is bigger.

**OPON\_N[7:0]:** Specify the Normal mode valid source OP output period in 1-line driving period.

**OPON\_I[7:0]:** Specify the IDLE mode valid source OP output period in 1-line driving period.

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**6.39 Power control internal used (PAGE0 -REAh~ECh)**

|            |            |         |         |         |         |         |         |        |        |
|------------|------------|---------|---------|---------|---------|---------|---------|--------|--------|
| <b>R/W</b> | <b>DNC</b> | D7      | D6      | D5      | D4      | D3      | D2      | D1     | D0     |
| W          | 1          | PTB A15 | PTB A14 | PTB A13 | PTB A12 | PTB A11 | PTB A10 | PTA B9 | PTB A8 |
| R          | 1          | PTB A15 | PTB A14 | PTB A13 | PTB A12 | PTB A11 | PTB A10 | PTA B9 | PTB A8 |

Figure 6.100: Power control internal used (1) register (PAGE0 -REAh)

|            |            |        |        |        |        |        |        |        |        |
|------------|------------|--------|--------|--------|--------|--------|--------|--------|--------|
| <b>R/W</b> | <b>DNC</b> | D7     | D6     | D5     | D4     | D3     | D2     | D1     | D0     |
| W          | 1          | PTB A7 | PTB A6 | PTB A5 | PTB A4 | PTB A3 | PTB A2 | PTB A1 | PTB A0 |
| R          | 1          | PTB A7 | PTB A6 | PTB A5 | PTB A4 | PTB A3 | PTB A2 | PTB A1 | PTB A0 |

Figure 6.101: Power control internal used (2) register (PAGE0 -REBh)

|            |            |         |         |         |         |         |         |        |        |
|------------|------------|---------|---------|---------|---------|---------|---------|--------|--------|
| <b>R/W</b> | <b>DNC</b> | D7      | D6      | D5      | D4      | D3      | D2      | D1     | D0     |
| W          | 1          | STB A15 | STB A14 | STB A13 | STB A12 | STB A11 | STB A10 | STA B9 | STB A8 |
| R          | 1          | STB A15 | STB A14 | STB A13 | STB A12 | STB A11 | STB A10 | STA B9 | STB A8 |

Figure 6.102: Source control internal used (1) register (PAGE0 -RECh)

|            |            |        |        |        |        |        |        |        |        |
|------------|------------|--------|--------|--------|--------|--------|--------|--------|--------|
| <b>R/W</b> | <b>DNC</b> | D7     | D6     | D5     | D4     | D3     | D2     | D1     | D0     |
| W          | 1          | STB A7 | STB A6 | STB A5 | STB A4 | STB A3 | STB A2 | STB A1 | STB A0 |
| R          | 1          | STB A7 | STB A6 | STB A5 | STB A4 | STB A3 | STB A2 | STB A1 | STB A0 |

Figure 6.103: Source control internal used (2) register (PAGE0 -REDh)

These commands are internal used.

**PTBA[15:0]:** Power control internal used.

**STBA[15:0]:** Source Power control internal used.

**6.40 Command page select register (RFFh)**

|            |            |     |     |     |     |     |     |            |            |
|------------|------------|-----|-----|-----|-----|-----|-----|------------|------------|
| <b>R/W</b> | <b>DNC</b> | RB7 | RB6 | RB5 | RB4 | RB3 | RB2 | RB1        | RB0        |
| W          | 1          | *   | *   | *   | *   | *   | *   | PAGE_SEL 1 | PAGE_SEL 0 |
| R          | 1          | 0   | 0   | 0   | 0   | 0   | 0   | PAGE_SEL 1 | PAGE_SEL 0 |

Figure 6.104: Command page select register (RFFh)

**PAGE\_SEL[1:0]:** Command set page select.

| PAGE_SEL1 | PAGE_SEL0 | Command Page |
|-----------|-----------|--------------|
| 0         | 0         | Page 0       |
| 0         | 1         | Page 1       |

6.41 DGC Control register (PAGE1 -00h)

|     |     |     |     |     |     |     |     |     |        |
|-----|-----|-----|-----|-----|-----|-----|-----|-----|--------|
| R/W | DNC | RB7 | RB6 | RB5 | RB4 | RB3 | RB2 | RB1 | RB0    |
| W   | 1   | *   | *   | *   | *   | *   | *   | *   | DGC_EN |
| R   | 1   | 0   | 0   | 0   | 0   | 0   | 0   | 0   | DGC_EN |

Figure 6.105: DGC control register (PAGE1 -00h)

**DGC\_EN:** Digital gamma correction enable.  
 0: Disable  
 1: Enable

6.42 DGC LUT register (PAGE1 -01h~63h)

|     |     |     |     |     |     |     |     |     |     |
|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|
| R/W | DNC | RB7 | RB6 | RB5 | RB4 | RB3 | RB2 | RB1 | RB0 |
| W   | 1   | D7  | D6  | D5  | D4  | D3  | D2  | D1  | D0  |
| R   | 1   | D7  | D6  | D5  | D4  | D3  | D2  | D1  | D0  |

Figure 6.106: DGC LUT register (PAGE1 -01h~63h)

There are 99 bytes DGC LUT to set R, G, B gamma independently. When DGC\_EN=1, R, G, B gamma will mapping V0, V2, V4, ..., V60, V62, V63 voltage to the LUT register setting gray level voltage.  $V(2N+1) = (V(2N) + V(2N+2))/2$  (N=0~30).

| Parameter | Input (6 bit) | D7   | D6   | D5   | D4   | D3   | D2   | D1   | D0   | Default | Gray Mapping |
|-----------|---------------|------|------|------|------|------|------|------|------|---------|--------------|
| 1st       | R00h          | R007 | R006 | R005 | R004 | R003 | R002 | R001 | R000 | 00h     | R_V0         |
| 2nd       | R02h          | R017 | R016 | R015 | R014 | R013 | R012 | R011 | R010 | 08h     | R_V2         |
| 3rd       | R04h          | R027 | R026 | R025 | R024 | R023 | R022 | R021 | R020 | 10h     | R_V4         |
|           | ⋮             | ⋮    | ⋮    | ⋮    | ⋮    | ⋮    | ⋮    | ⋮    | ⋮    | ⋮       | ⋮            |
| 32nd      | R62h          | R317 | R316 | R315 | R314 | R313 | R312 | R311 | R310 | F8h     | R_V62        |
| 33rd      | R63h          | R327 | R326 | R325 | R324 | R323 | R322 | R321 | R320 | FCh     | R_V63        |
| 34th      | G00h          | G007 | G006 | G005 | G004 | G003 | G002 | G001 | G000 | 00h     | G_V0         |
| 35th      | G02h          | G017 | G016 | G015 | G014 | G013 | G012 | G011 | G010 | 08h     | G_V2         |
| 36th      | G04h          | G027 | G026 | G025 | G024 | G023 | G022 | G021 | G020 | 10h     | G_V4         |
|           | ⋮             | ⋮    | ⋮    | ⋮    | ⋮    | ⋮    | ⋮    | ⋮    | ⋮    | ⋮       | ⋮            |
| 65th      | G62h          | G317 | G316 | G315 | G314 | G313 | G312 | G311 | G310 | F8h     | G_V62        |
| 66th      | G63h          | G327 | G326 | G325 | G324 | G323 | G322 | G321 | G320 | FCh     | G_V63        |
| 67th      | B00h          | B007 | B006 | B005 | B004 | B003 | B002 | B001 | B000 | 00h     | B_V0         |
| 68th      | B02h          | B017 | B016 | B015 | B014 | B013 | B012 | B011 | B010 | 08h     | B_V2         |
| 69th      | B04h          | B027 | B026 | B025 | B024 | B023 | B022 | B021 | B020 | 10h     | B_V4         |
|           | ⋮             | ⋮    | ⋮    | ⋮    | ⋮    | ⋮    | ⋮    | ⋮    | ⋮    | ⋮       | ⋮            |
| 98th      | B62h          | B317 | B316 | B315 | B314 | B313 | B312 | B311 | B310 | F8h     | B_V62        |
| 99th      | B63h          | B327 | B326 | B325 | B324 | B323 | B322 | B321 | B320 | FCh     | B_V63        |

6.43 CABC control 5~7 register (PAGE1 – RC3h, RC5h, RC7h)

| R/W | DNC | RB7        | RB6         | RB5         | RB4         | RB3 | RB2 | RB1        | RB0 |
|-----|-----|------------|-------------|-------------|-------------|-----|-----|------------|-----|
| W   | 1   | BC_C<br>TL | PWM<br>DIV2 | PWM<br>DIV1 | PWM<br>DIV0 | 1   | 1   | INPL<br>US | 1   |
| R   | 1   | BC_C<br>TL | PWM<br>DIV2 | PWM<br>DIV1 | PWM<br>DIV0 | 1   | 1   | INPL<br>US | 1   |

Figure 6.107: CABC control 5 (PAGE1 – RC3h)

| R/W | DNC | RB7                 | RB6                 | RB5                 | RB4                 | RB3                 | RB2                 | RB1                 | RB0                 |
|-----|-----|---------------------|---------------------|---------------------|---------------------|---------------------|---------------------|---------------------|---------------------|
| W   | 1   | PWM_<br>PERIO<br>D7 | PWM_<br>PERIO<br>D6 | PWM_<br>PERIO<br>D5 | PWM_<br>PERIO<br>D4 | PWM_<br>PERIO<br>D3 | PWM_<br>PERIO<br>D2 | PWM_<br>PERIO<br>D1 | PWM_<br>PERIO<br>D0 |
| R   | 1   | PWM_<br>PERIO<br>D7 | PWM_<br>PERIO<br>D6 | PWM_<br>PERIO<br>D5 | PWM_<br>PERIO<br>D4 | PWM_<br>PERIO<br>D3 | PWM_<br>PERIO<br>D2 | PWM_<br>PERIO<br>D1 | PWM_<br>PERIO<br>D0 |

Figure 6.108: CABC control 6 (PAGE1 – RC5h)

| R/W | DNC | RB7 | RB6                | RB5            | RB4            | RB3            | RB2            | RB1            | RB0            |
|-----|-----|-----|--------------------|----------------|----------------|----------------|----------------|----------------|----------------|
| W   | 1   | 0   | DIM_F<br>RAME<br>6 | DIM_F<br>RAME5 | DIM_F<br>RAME4 | DIM_F<br>RAME3 | DIM_F<br>RAME2 | DIM_F<br>RAME1 | DIM_F<br>RAME0 |
| R   | 1   | 0   | DIM_F<br>RAME<br>6 | DIM_F<br>RAME5 | DIM_F<br>RAME4 | DIM_F<br>RAME3 | DIM_F<br>RAME2 | DIM_F<br>RAME1 | DIM_F<br>RAME0 |

Figure 6.109: CABC control 7 (PAGE1 – RC7h)

**BC\_CTL:** The control register for LED driver when IC needs enable signal.  
 '0': BC\_CTRL pin='L'  
 '1': BC\_CTRL pin='H'

**PWM\_DIV[2:0]:** Internal PWM\_CLK divider for CABC clock.

| PWM_DIV[2:0] | Divider     |
|--------------|-------------|
| 0            | PWM_CLK/1   |
| 1            | PWM_CLK/2   |
| 2            | PWM_CLK/4   |
| 3            | PWM_CLK/8   |
| 4            | PWM_CLK/16  |
| 5            | PWM_CLK/32  |
| 6            | PWM_CLK/64  |
| 7            | PWM_CLK/128 |

**Note:** PWM\_CLK is OSC frequency in system interface and DOTCLK in RGB interface.

**INVPULS:** The backlight PWM output polarity select.  
 '0', The backlight PWM output is low level active.  
 '1', The backlight PWM output is high level active.

**PWM\_PERIOD[7:0] :** The backlight PWM output period setting.  
 Backlight PWM output period = 1 / (PWM\_CLK / clock divider (PWMDIV)) x  
 (255x(PWM\_PERIOD[7:0]+1))

**DIM\_FRAME[6:0] :** Manual brightness setting dimming period.



**6.44 Gain select register 0~8 (PAGE1 – RCBh~D3h)**

| R/W | DNC | RB7 | RB6       | RB5       | RB4       | RB3       | RB2       | RB1       | RB0       |
|-----|-----|-----|-----------|-----------|-----------|-----------|-----------|-----------|-----------|
| W   | 1   | *   | DBG<br>06 | DBG<br>05 | DBG<br>04 | DBG<br>03 | DBG<br>02 | DBG<br>01 | DBG<br>00 |
| R   | 1   | 0   | DBG<br>06 | DBG<br>05 | DBG<br>04 | DBG<br>03 | DBG<br>02 | DBG<br>01 | DBG<br>00 |

**Figure 6.110: Gain select register 0 (PAGE1 – RCBh)**

| R/W | DNC | RB7 | RB6       | RB5       | RB4       | RB3       | RB2       | RB1       | RB0       |
|-----|-----|-----|-----------|-----------|-----------|-----------|-----------|-----------|-----------|
| W   | 1   | *   | DBG<br>16 | DBG<br>15 | DBG<br>14 | DBG<br>13 | DBG<br>12 | DBG<br>11 | DBG<br>10 |
| R   | 1   | 0   | DBG<br>16 | DBG<br>15 | DBG<br>14 | DBG<br>13 | DBG<br>12 | DBG<br>11 | DBG<br>10 |

**Figure 6.111: Gain select register 1 (PAGE1 – RCCh)**

| R/W | DNC | RB7 | RB6       | RB5       | RB4       | RB3       | RB2       | RB1       | RB0       |
|-----|-----|-----|-----------|-----------|-----------|-----------|-----------|-----------|-----------|
| W   | 1   | *   | DBG<br>26 | DBG<br>25 | DBG<br>24 | DBG<br>23 | DBG<br>22 | DBG<br>21 | DBG<br>20 |
| R   | 1   | 0   | DBG<br>26 | DBG<br>25 | DBG<br>24 | DBG<br>23 | DBG<br>22 | DBG<br>21 | DBG<br>20 |

**Figure 6.112: Gain select register 2 (PAGE1 – RCDh)**

| R/W | DNC | RB7 | RB6       | RB5       | RB4       | RB3       | RB2       | RB1       | RB0       |
|-----|-----|-----|-----------|-----------|-----------|-----------|-----------|-----------|-----------|
| W   | 1   | *   | DBG<br>36 | DBG<br>35 | DBG<br>34 | DBG<br>33 | DBG<br>32 | DBG<br>31 | DBG<br>30 |
| R   | 1   | 0   | DBG<br>36 | DBG<br>35 | DBG<br>34 | DBG<br>33 | DBG<br>32 | DBG<br>31 | DBG<br>30 |

**Figure 6.113: Gain select register 3 (PAGE1 – RCEh)**

| R/W | DNC | RB7 | RB6       | RB5       | RB4       | RB3       | RB2       | RB1       | RB0       |
|-----|-----|-----|-----------|-----------|-----------|-----------|-----------|-----------|-----------|
| W   | 1   | *   | DBG<br>46 | DBG<br>45 | DBG<br>44 | DBG<br>43 | DBG<br>42 | DBG<br>41 | DBG<br>40 |
| R   | 1   | 0   | DBG<br>46 | DBG<br>45 | DBG<br>44 | DBG<br>43 | DBG<br>42 | DBG<br>41 | DBG<br>40 |

**Figure 6.114: Gain select register 4 (PAGE1 – RCFh)**

| R/W | DNC | RB7 | RB6       | RB5       | RB4       | RB3       | RB2       | RB1       | RB0       |
|-----|-----|-----|-----------|-----------|-----------|-----------|-----------|-----------|-----------|
| W   | 1   | *   | DBG<br>56 | DBG<br>55 | DBG<br>54 | DBG<br>53 | DBG<br>52 | DBG<br>51 | DBG<br>50 |
| R   | 1   | 0   | DBG<br>56 | DBG<br>55 | DBG<br>54 | DBG<br>53 | DBG<br>52 | DBG<br>51 | DBG<br>50 |

**Figure 6.115: Gain select register 5 (PAGE1 – RD0h)**

| R/W | DNC | RB7 | RB6       | RB5       | RB4       | RB3       | RB2       | RB1       | RB0       |
|-----|-----|-----|-----------|-----------|-----------|-----------|-----------|-----------|-----------|
| W   | 1   | *   | DBG<br>66 | DBG<br>65 | DBG<br>64 | DBG<br>63 | DBG<br>62 | DBG<br>61 | DBG<br>60 |
| R   | 1   | 0   | DBG<br>66 | DBG<br>65 | DBG<br>64 | DBG<br>63 | DBG<br>62 | DBG<br>61 | DBG<br>60 |

Figure 6.116: Gain select register 6 (PAGE1 – RD1h)

| R/W | DNC | RB7 | RB6       | RB5       | RB4       | RB3       | RB2       | RB1       | RB0       |
|-----|-----|-----|-----------|-----------|-----------|-----------|-----------|-----------|-----------|
| W   | 1   | *   | DBG<br>76 | DBG<br>75 | DBG<br>74 | DBG<br>73 | DBG<br>72 | DBG<br>71 | DBG<br>70 |
| R   | 1   | 0   | DBG<br>76 | DBG<br>75 | DBG<br>74 | DBG<br>73 | DBG<br>72 | DBG<br>71 | DBG<br>70 |

Figure 6.117: Gain select register 7 (PAGE1 – RD2h)

| R/W | DNC | RB7 | RB6       | RB5       | RB4       | RB3       | RB2       | RB1       | RB0       |
|-----|-----|-----|-----------|-----------|-----------|-----------|-----------|-----------|-----------|
| W   | 1   | *   | DBG<br>86 | DBG<br>85 | DBG<br>84 | DBG<br>83 | DBG<br>82 | DBG<br>81 | DBG<br>80 |
| R   | 1   | 0   | DBG<br>86 | DBG<br>85 | DBG<br>84 | DBG<br>83 | DBG<br>82 | DBG<br>81 | DBG<br>80 |

Figure 6.118: Gain select register 8 (PAGE1 – RD3h)

**DBG0~8[6:0] : Gain select register 0~8**

| DBGX | Duty      | DBGX      | Duty      | DBGX | Duty   |
|------|-----------|-----------|-----------|------|--------|
| 20   | 100.00%   | 30        | 66.67%    | 40   | 49.80% |
| 21   | 96.86%    | 31        | 65.10%    |      |        |
| 22   | 94.12%    | 32        | 63.92%    |      |        |
| 23   | 91.37%    | 33        | 62.75%    |      |        |
| 24   | 89.02%    | 34        | 61.57%    |      |        |
| 25   | 86.27%    | 35        | 60.39%    |      |        |
| 26   | 84.31%    | 36        | 59.22%    |      |        |
| 27   | 81.96%    | 37        | 58.04%    |      |        |
| 28   | 80.00%    | 38        | 56.86%    |      |        |
| 29   | 78.04%    | 39        | 56.08%    |      |        |
| 2A   | 76.08%    | 3A        | 54.90%    |      |        |
| 2B   | 74.51%    | 3B        | 54.12%    |      |        |
| 2C   | 72.55%    | 3C        | 53.33%    |      |        |
| 2D   | 70.98%    | 3D        | 52.16%    |      |        |
| 2E   | 69.41%    | 3E        | 51.37%    |      |        |
| 2F   | 67.84%    | 3F        | 50.59%    |      |        |
|      | <b>UI</b> | <b>ST</b> | <b>MV</b> |      |        |
| DBG0 | 24        | 40        | 40        |      |        |
| DBG1 | 24        | 3C        | 3C        |      |        |
| DBG2 | 24        | 38        | 38        |      |        |
| DBG3 | 23        | 34        | 34        |      |        |
| DBG4 | 23        | 33        | 33        |      |        |
| DBG5 | 23        | 32        | 32        |      |        |
| DBG6 | 22        | 2B        | 2D        |      |        |
| DBG7 | 22        | 24        | 2B        |      |        |
| DBG8 | 22        | 22        | 28        |      |        |

### 7. Layout Recommendation

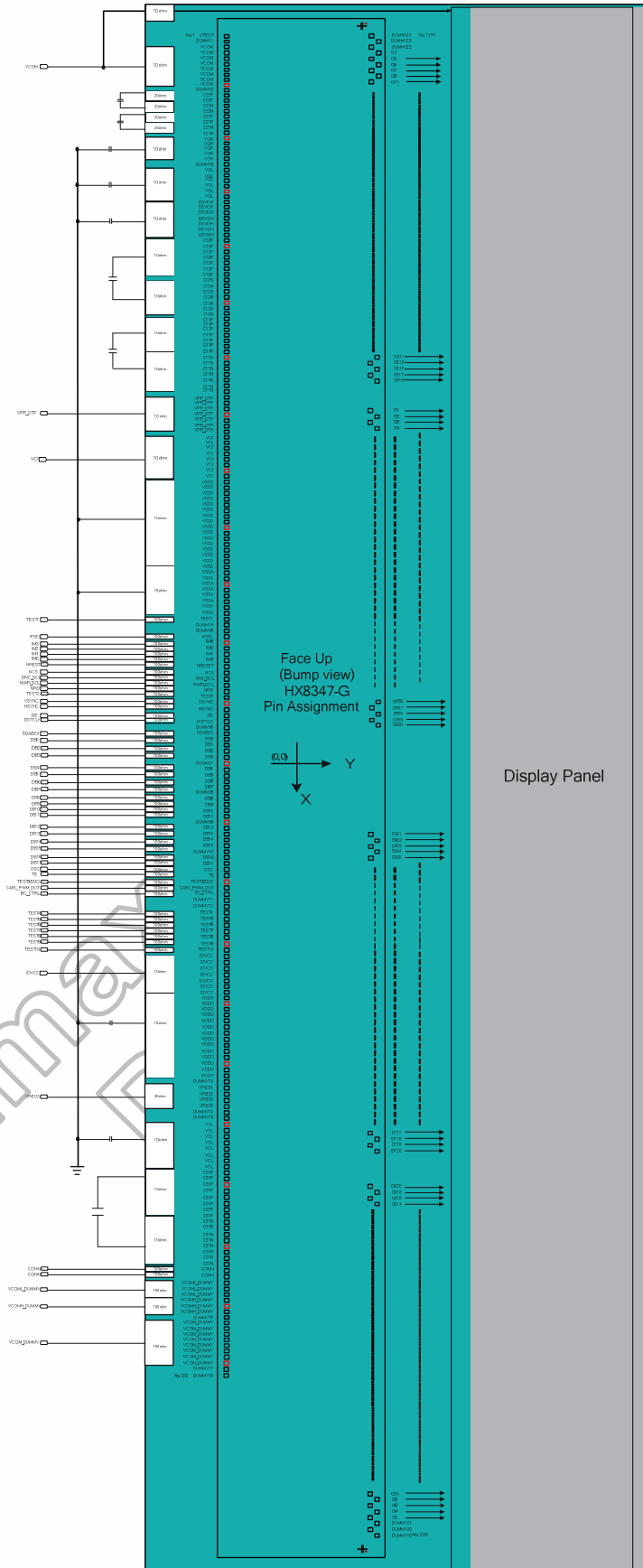


Figure 7.1: Layout recommendation of HX8347-G

**7.1 Maximum layout resistance**

| Name                              | Type                 | Maximum Series Resistance | Unit |
|-----------------------------------|----------------------|---------------------------|------|
| IOVCC                             | Power supply         | 10                        | Ω    |
| VCI                               | Power supply         | 10                        | Ω    |
| VSSA,VSSC                         | Power supply         | 10                        | Ω    |
| VSSD                              | Power supply         | 10                        | Ω    |
| VPP_OTP                           | Power supply         | 10                        | Ω    |
| OSC                               | Input                | 100                       | Ω    |
| IM[3:0], IFSEL                    | Input                | 100                       | Ω    |
| NRD_E, NWR_RNW, DNC_SCL, NCS, SDA | Input                | 100                       | Ω    |
| NRESET                            | Input                | 100                       | Ω    |
| TE, CABP_PWM_OUT,BC_CTRL          | Output               | 100                       | Ω    |
| DB[17:0],                         | I/O                  | 100                       | Ω    |
| DOTCLK, DE, VSYNC, HSYNC          | Input                | 100                       | Ω    |
| VGH                               | Capacitor connection | 10                        | Ω    |
| VGL                               | Capacitor connection | 10                        | Ω    |
| VCL                               | Capacitor connection | 10                        | Ω    |
| DDVDH                             | Capacitor connection | 10                        | Ω    |
| VDDD                              | Capacitor connection | 10                        | Ω    |
| VREG1                             | Capacitor connection | 50                        | Ω    |
| C11P, C11N, C12P, C12N            | Capacitor connection | 10                        | Ω    |
| C31P, C12N                        | Capacitor connection | 10                        | Ω    |
| C21P, C21N                        | Capacitor connection | 15                        | Ω    |
| C22P, C22N                        | Capacitor connection | 15                        | Ω    |
| TEST[10:1]                        | Input                | 100                       | Ω    |
| VCOMH_DUMMY, VCOML_DUMMY,DUMMY    | Dummy                | 100                       | Ω    |
| VTEST,VMONI                       | Test Pin             | 100                       | Ω    |

**7.2 External components connection**

| Capacitor   | Recommended voltage | Capacity                      |
|-------------|---------------------|-------------------------------|
| C1 (C11P/N) | 6V                  | 1 $\mu$ F (B characteristics) |
| C2 (C12P/N) | 6V                  | 1 $\mu$ F (B characteristics) |
| C3 (DDVDH)  | 10V                 | 1 $\mu$ F (B characteristics) |
| C4 (C21P/N) | 10V                 | 1 $\mu$ F (B characteristics) |
| C5 (C22P/N) | 10V                 | 1 $\mu$ F (B characteristics) |
| C6 (VGH)    | 25V                 | 1 $\mu$ F (B characteristics) |
| C7 (VGL)    | 16V                 | 1 $\mu$ F (B characteristics) |
| C8 (C31P/N) | 6V                  | 1 $\mu$ F (B characteristics) |
| C9 (VCL)    | 6V                  | 1 $\mu$ F (B characteristics) |
| C10(VDDD)   | 6V                  | 1 $\mu$ F (B characteristics) |

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## 8. Electrical Characteristic

### 8.1 Absolute maximum ratings

| Item                   | Symbol          | Unit | Spec. |      |           | Note                     |
|------------------------|-----------------|------|-------|------|-----------|--------------------------|
|                        |                 |      | Min.  | Typ. | Max.      |                          |
| Power Supply Voltage 1 | IOVCC~VSSD      | V    | -0.3  | -    | +4.6      | Note <sup>(1),(2)</sup>  |
| Power Supply Voltage 2 | VCI ~ VSSA      | V    | -0.3  | -    | +4.6      | Note <sup>(3)</sup>      |
| Power Supply Voltage 3 | DDVDH ~ VSSA    | V    | -0.3  | -    | +6.6      | Note <sup>(4)</sup>      |
| Power Supply Voltage 4 | VSSA ~ VCL      | V    | -0.3  | -    | +4.6      | Note <sup>(5)</sup>      |
| Power Supply Voltage 5 | DDVDH ~ VCL     | V    | -0.3  | -    | +9        | Note <sup>(6)</sup>      |
| Power Supply Voltage 6 | VGH ~ VSSA      | V    | -0.3  | -    | +18.5     | Note <sup>(7)</sup>      |
| Power Supply Voltage 7 | VSSA ~ VGL      | V    | -16.5 | -    | 0         | Note <sup>(8)</sup>      |
| Logic Input Voltage    | V <sub>IN</sub> | V    | -0.3  | -    | IOVCC+0.5 | -                        |
| Logic Output Voltage   | V <sub>o</sub>  | V    | -0.3  | -    | IOVCC+0.5 | -                        |
| Operating Temperature  | Topr            | °C   | -40   | -    | +85       | Note <sup>(9),(10)</sup> |
| Storage Temperature    | Tstg            | °C   | -55   | -    | +110      | Note <sup>(9),(10)</sup> |

**Note:** (1) IOVCC, VSSD must be maintained.

(2) To make sure IOVCC ≥ VSSD.

(3) To make sure VCI ≥ VSSA.

(4) To make sure DDVDH ≥ VSSA.

(5) To make sure VSSA ≥ VCL.

(6) To make sure DDVDH ≥ VCL.

(7) To make sure VGH ≥ VSSA.

(8) To make sure VSSA ≥ VGL

VGH +|VGL| < 32V

(9) For die and wafer products, specified up to +85°C.

(10) This temperature specifications apply to the TCP package.

**Table 8.1: Absolute maximum ratings**

### 8.2 ESD protection level

| Mode             | Test Condition   | Protection Level | Unit |
|------------------|------------------|------------------|------|
| Human Body Model | C=100pF, R=1.5kΩ | ±2.0K            | V    |
| Machine Model    | C=200pF, R=0.0Ω  | ±200             | V    |

**Table 8.2: ESD protection level**

## 8.3 DC characteristics

| Parameter                                  | Symbol  | Conditions  | Spec.    |        |           | Unit |
|--|---------|---|----------|--------|-----------|------|
|  |         |   | Min.     | Typ.   | Max.      |      |
| <b>Power &amp; Operating Voltages</b>      |         |   |          |        |           |      |
| IO Operating voltage                       | IOVCC   | I/O supply voltage  | 1.65     | 1.8    | 3.3       | V    |
| Driver Operating voltage                   | VCI     | Operation voltage   | 2.3      | 2.8    | 3.3       |      |
| Source Drive Voltage                       | VREG1   | Triple Pump   | 3.3      | 4.65   | 4.8       |      |
|  | VREG1   | Dual Pump   | 3.3      | 4.65   | 5.8       |      |
| Gate Drive High Voltage                    | VGH     | IVGH=100μA<br>(Typ:BT=001) VCI=2.8<br>Dual Pump               | 9.5      | 14.25  | -         |      |
|  |         | IVGH=100uA<br>(Typ:BT=001)<br>VCI=2.8<br>Triple Pump          | 11.6     | 17.39  | -         |      |
| Gate Drive Low Voltage                     | VGL     | IVGL=100μA<br>(Typ:BT=001) VCI=2.8<br>Dual Pump               | -6.85    | -9.5   | -         |      |
|  |         | IVGL=100μA<br>(Typ:BT=001)<br>VCI=2.8<br>Triple Pump          | -8.46    | -11.59 | -         |      |
| Drive Supply Voltage                       | VGH-VGL | -   | -        | -      | 30        |      |
| <b>Input / Output</b>                      |         |   |          |        |           |      |
| High level input voltage                   | VIH     | -   | 0.7IOVCC | -      | IOVCC     | V    |
| Low level input voltage                    | VIL     | -   | VSSD     | -      | 0.3IOVCC  |      |
| High level output voltage                  | VOH     | IOH=-1.0mA  | 0.8IOVCC | -      | IOVCC     |      |
| Low level output voltage                   | VOL     | IOL=+1.0mA  | VSSD     | -      | 0.2IOVCC  |      |
| Input leakage current                      | IIL     | -   | -1       | -      | 1         | μA   |
| Oscillator frequency                       | fOSC    | Frame rate at<br>65hz,default Vs and Hs<br>setting<br>TA=25°C | 2.61     | 2.75   | 2.89      | MHz  |
| <b>Booster(VCI=2.8V)</b>                   |         |   |          |        |           |      |
| DDVDH boost voltage1                       | DDVDH   | Dual Pump<br>IDDVDH=1mA                                       | 4.8      | 5.0    | 5.2       | V    |
|  |         | Triple Pump<br>IDDVDH=1mA                                     | 5.9      | 6.1    | 6.3       |      |
| VCL boost voltage                          | VCL     | ICL=-300μA  | -2.5     | -2.65  | 2.75      |      |
| <b>VCOM Generator(VCI=2.8V)</b>            |         |   |          |        |           |      |
| VCOM amplitude                             | VCOM    | No load,<br>Dual Pump   | 2.5      | 4.4    | 7.3       | V    |
|  |         | No load<br>Triple Pump  | 2.5      | 4.4    | 8.3       | V    |
| VCOM high level                            | VCOMH   | No load<br>Dual Pump  | 2.5      | 3.205  | 4.8       | V    |
|  |         | No load<br>Triple Pump  | 2.5      | 3.205  | 5.8       | V    |
| VCOM low level                             | VCOML   | No load   | -2.5     | -1.195 | VSSD      | V    |
| <b>Source Driver(Typ:TA=25°C VCI=2.8v)</b> |         |   |          |        |           |      |
| Output voltage deviation<br>(mean value)   | DVOS    | VSSD+1.0 ~ VREG1-1.0  | -        | +/-10  | +/-20     | mV   |
|  |         | VSSD+0.1V ~<br>VSSD+1.0<br>VREG1-1.0 ~<br>VREG1-0.1V          | -        | +/-30  | +/-50     | mV   |
|  |         |   |          |        |           |      |
| Output voltage range                       | VOS     | -   | 0.1      | -      | DDVDH-0.1 | V    |
| Output offset voltage                      | Voff    | -   | -        | +/-30  | +/-50     | mV   |

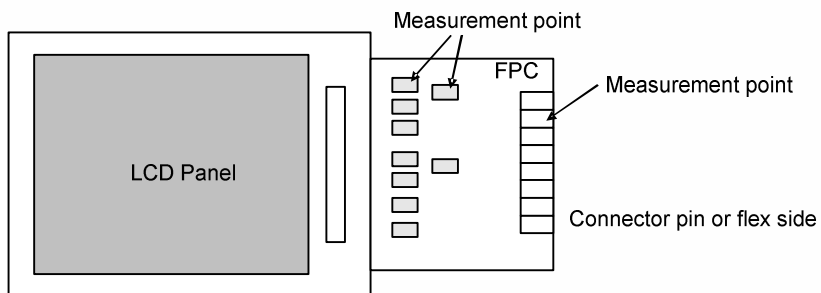


# >> HX8347-G(T)

240RGB x 320 dot, 262K color, TFT Mobile Single Chip Driver



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## 8.4 Current consumption

| Host I/F                  | Mode of operation                       | Frame Frequency | Inversion Mode | Image  | Memory Data Access Control (MY:MX:MV) | Current Consumption |            |            |            |
|---------------------------|---|-----------------|----------------|--|---------------------------------------|---------------------|------------|------------|------------|
|                           |   |                 |                |  |                                       | Typical             |            | Worst Case |            |
|                           |   |                 |                |  |                                       | VCI (mA)            | IOVCC (mA) | VCI (mA)   | IOVCC (mA) |
| Host interface NOT active | Normal Mode On                          | 60Hz            | 1-line         | Black  | X;X;X                                 | 3.48                | 0.21       | 3.85       | 0.33       |
|                           |   |                 | 1-line         | 1x1 checker board                            | X;X;X                                 | 2.82                | 0.21       | 3.06       | 0.33       |
|                           |   |                 | 1-line         | 4x4 checker board                            | X;X;X                                 | 2.76                | 0.33       | 3.12       | 0.42       |
|                           |   |                 | 1-line         | Gray_Scale Top to Bottom                     | X;X;X                                 | 2.57                | 0.22       | 3.00       | 0.33       |
|                           |   |                 | 1-line         | 20B80W                                       | X;X;X                                 | 3.05                | 0.21       | 3.50       | 0.32       |
|                           | Idle Mode On                            | 60Hz            | 1-line         | 20B80W                                       | X;X;X                                 | 2.40                | 0.17       | 2.74       | 0.25       |
|                           | Partial Mode On (48 lines)              | 60Hz            | 1-line         | Grey Levels                                  | X;X;X                                 | 0.86                | 0.11       | 1.35       | 0.18       |
|                           | Partial Mode On (48 lines) Idle Mode On | 60Hz            | 1-line         | 8x8 checker board                            | X;X;X                                 | 0.99                | 0.09       | 1.12       | 0.15       |
|                           |   |                 | 1-line         | Worst pattern                                | X;X;X                                 | 1.01                | 0.09       | 1.20       | 0.15       |
|                           | Standby Mode                            | N/A             | N/A            | N/A  | X;X;X                                 | 0.00059             | 0.00452    | 0.010      | 0.080      |
| Deep Standby Mode         | N/A                                     | N/A             | N/A            | X;X;X  | 0.0005                                | 0.001               | 0.005      | 0.010      |            |
| Host interface active     | Normal Mode On                          | 60Hz            | 1-line         | 262k Colors Worst pattern CPU Access @ 15fps | 0;0;0                                 | 3.29                | 0.98       | 3.89       | 1.30       |
|                           |   |                 |                |  | 0;0;1                                 | 3.29                | 0.98       | 3.89       | 1.30       |
|                           |   |                 |                |  | 0;1;0                                 | 3.29                | 0.98       | 3.89       | 1.30       |
|                           |   |                 |                |  | 0;1;1                                 | 3.29                | 0.98       | 3.89       | 1.30       |
|                           |   |                 |                |  | 1;0;0                                 | 3.29                | 0.98       | 3.89       | 1.30       |
|                           |   |                 |                |  | 1;0;1                                 | 3.29                | 0.98       | 3.89       | 1.30       |
|                           |   |                 |                |  | 1;1;0                                 | 3.29                | 0.98       | 3.89       | 1.30       |
|                           |   |                 |                |  | 1;1;1                                 | 3.29                | 0.98       | 3.89       | 1.30       |
|                           |   |                 |                | 262k Colors Worst pattern CPU Access @ 25fps | 0;0;0                                 | 3.28                | 1.54       | 3.88       | 1.88       |
|                           |   |                 |                |  | 0;0;1                                 | 3.28                | 1.54       | 3.88       | 1.88       |
|                           |   |                 |                |  | 0;1;0                                 | 3.28                | 1.54       | 3.88       | 1.88       |
|                           |   |                 |                |  | 0;1;1                                 | 3.28                | 1.54       | 3.88       | 1.88       |
|                           |   |                 |                |  | 1;0;0                                 | 3.28                | 1.54       | 3.88       | 1.88       |
|                           |   |                 |                |  | 1;0;1                                 | 3.28                | 1.54       | 3.88       | 1.88       |
|                           |   |                 |                |  | 1;1;0                                 | 3.28                | 1.54       | 3.88       | 1.88       |
|                           |   |                 |                |  | 1;1;1                                 | 3.28                | 1.54       | 3.88       | 1.88       |

Table 8.3: Current consumption

Typical Case:

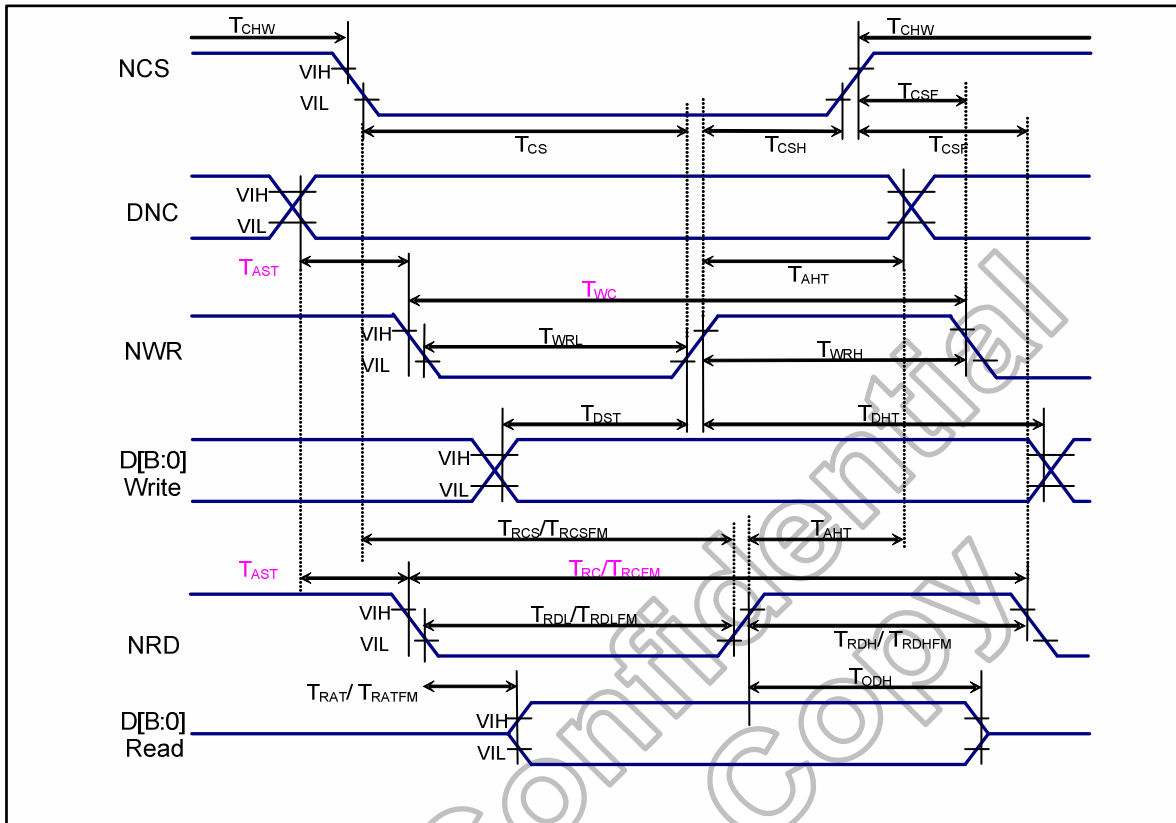
T<sub>A</sub> = 25oC  
 IOVCC=1.8V  
 VCI = 2.8V  
 CMO 2.6" panel

Worst Case:

T<sub>A</sub> = -30 to 70oC  
 IOVCC = 1.65V to 1.95V  
 VCI = 2.3V to 3.3V  
 Includes Process Variance.

**8.5 AC characteristics**

**8.5.1 Parallel interface characteristics (8080-series MPU)**

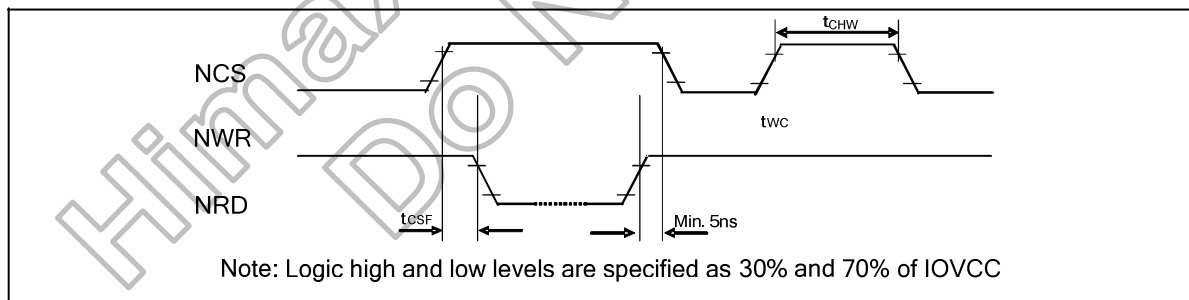
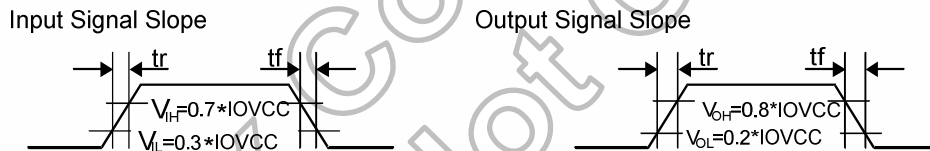


**Figure 8.1: Parallel interface characteristics (8080-series MPU)**

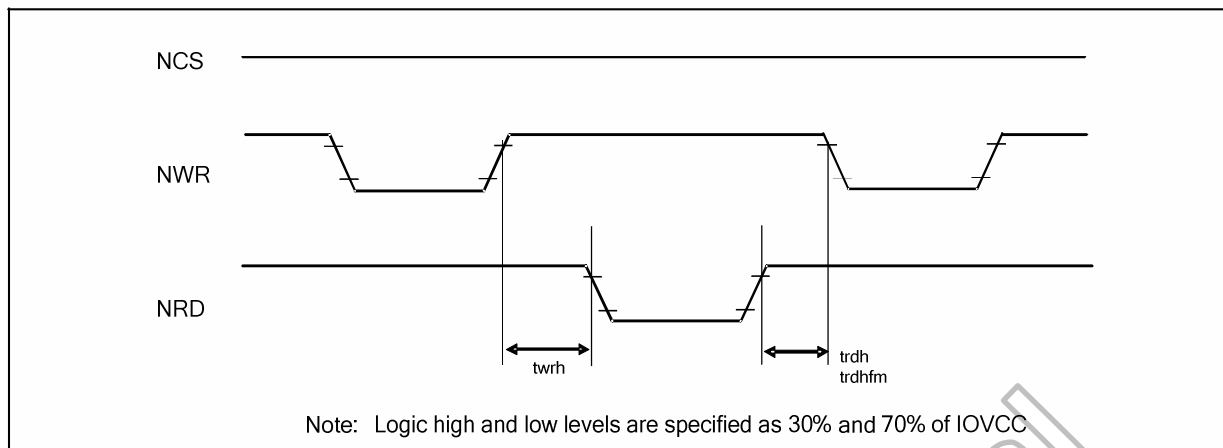
(VSSA=0V, IOVCC=1.65V to 3.3V, VCI=2.3V to 3.3V, T<sub>A</sub> = -30 to 70° C)

| Signal      | Symbol | Parameter                                 | Spec. |     |      | Unit | Description                               |
|-------------|--------|---|-------|-----|------|------|---|
|             |        |   | Min.  | Typ | Max. |      |   |
| DNC_SCL     | tAST   | Address setup time                        | 10    | -   | -    | ns   | -   |
|             | tAHT   | Address hold time (Write/Read)            | 10    | -   | -    |      |   |
| NCS         | tCHW   | Chip select "H" pulse width               | 0     | -   | -    | ns   | -   |
|             | tCS    | Chip select setup time (Write)            | 15    | -   | -    |      |   |
|             | tRCS   | Chip select setup time (Read ID)          | 45    | -   | -    |      |   |
|             | tRCSFM | Chip select setup time (Read FM)          | 355   | -   | -    |      |   |
|             | tCSF   | Chip select wait time (Write/Read)        | 10    | -   | -    |      |   |
|             | tCSH   | Chip select hold time                     | 10    | -   | -    |      |   |
| NWR_SCL     | tWC    | Write cycle (1 pixel for one write)       | 100   | -   | -    | ns   | -   |
|             | tWC    | Write cycle (1 pixel for 2 or 3 write)    | 50    | -   | -    |      |   |
|             | tWRH   | Control pulse "H" duration                | 15    | -   | -    |      |   |
|             | tWRL   | Control pulse "L" duration                | 15    | -   | -    |      |   |
| NRD(ID)     | tRC    | Read cycle (ID)                           | 160   | -   | -    | ns   | When read ID data                         |
|             | tRDH   | Control pulse "H" duration (ID)           | 90    | -   | -    |      |   |
|             | tRDL   | Control pulse "L" duration (ID)           | 45    | -   | -    |      |   |
| NRD(FM)     | tRCFM  | Read cycle (FM) ( 1 pixel for one read)   | 600   | -   | -    | ns   | When read from frame memory               |
|             | tRCFM  | Read cycle (FM) (1 pixel for 2 or 3 read) | 400   | -   | -    |      |   |
|             | tRDHFM | Control pulse "H" duration (FM)           | 90    | -   | -    |      |   |
|             | tRDLFM | Control pulse "L" duration (FM)           | 355   | -   | -    |      |   |
| DB17 to DB0 | tDST   | Data setup time                           | 10    | -   | -    | ns   | For maximum CL=30pF<br>For minimum CL=8pF |
|             | tDHT   | Data hold time                            | 10    | -   | -    |      |   |
|             | tRAT   | Read access time (ID)                     | -     | -   | 100  |      |   |
|             | tRATFM | Read access time (FM)                     | -     | -   | 340  |      |   |
|             | tODH   | Output disable time                       | 20    | -   | 80   |      |   |

**Note:** The input signal rise time and fall time (tr, tf) is specified at 15 ns or less.  
Logic high and low levels are specified as 30% and 70% of IOVCC for Input signals.



**Figure 8.2: Chip select timing**



**Figure 8.3: Write to read and read to write timing**

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8.5.2 Serial interface characteristics

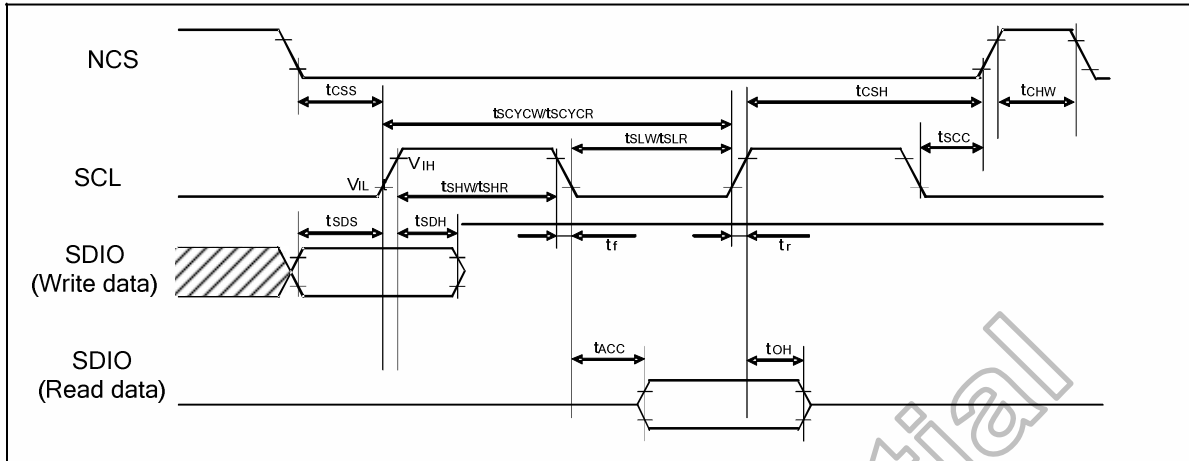


Figure 8.4: Serial interface characteristics

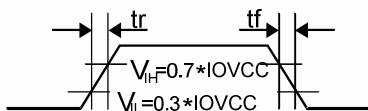
(VSSA=0V, IOVCC=1.65V to 3.3V, VCI=2.3V to 3.3V, TA=-30 to 70° C)

| Parameter                   | Symbol | Conditions                                    | Spec. |      |      | Unit |
|-----------------------------|--------|---|-------|------|------|------|
|                             |        |   | Min.  | Typ. | Max. |      |
| Serial clock cycle (Write)  | tSCYCW |   | 33    | -    | -    |      |
| SCL "H" pulse width (Write) | tSHW   | SCL   | 10    | -    | -    | ns   |
| SCL "L" pulse width (Write) | tSLW   | SCL   | 10    | -    | -    | ns   |
| Data setup time (Write)     | tSDS   | SDIO  | 10    | -    | -    | ns   |
| Data hold time (Write)      | tSDH   | SDIO  | 10    | -    | -    | ns   |
| Serial clock cycle (Read)   | tSCYCR |   | 150   | -    | -    |      |
| SCL "H" pulse width (Read)  | tSHR   | SCL   | 60    | -    | -    | ns   |
| SCL "L" pulse width (Read)  | tSLR   | SCL   | 60    | -    | -    | ns   |
| Access Time                 | tACC   | SDI for maximum CL=30pF<br>For minimum CL=8pF | 10    | -    | 50   | ns   |
| Output disable time         | tOH    | SDO For maximum CL=30pF<br>For minimum CL=8pF | 15    | -    | 50   | ns   |
| SCL to Chip select          | tSCC   | SCL, NCS                                      | 20    | -    | -    | ns   |
| NCS "H" pulse width         | tCHW   | NCS   | 40    | -    | -    | ns   |
| Chip select setup time      | tCSS   | NCS   | 15    | -    | -    | ns   |
| Chip select hold time       | tCWH   | NCS   | 15    | -    | -    | ns   |

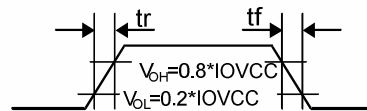
Note: The input signal rise time and fall time (tr, tf) is specified at 15 ns or less.

Logic high and low levels are specified as 30% and 70% of IOVCC for Input signals.

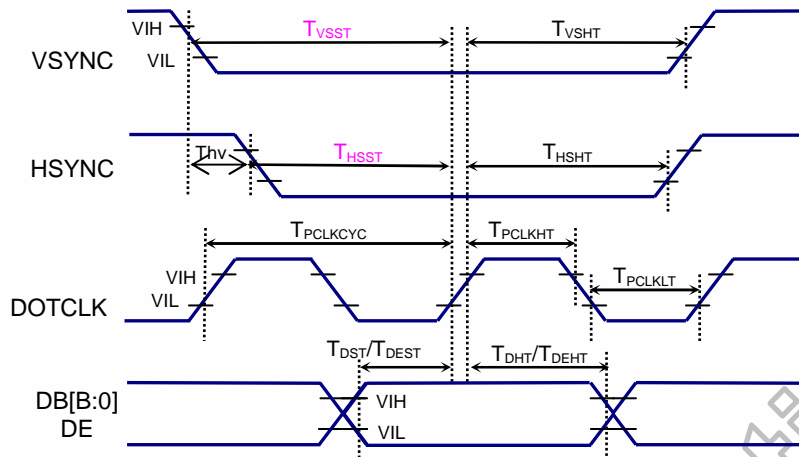
Input Signal Slope



Output Signal Slope



## 8.5.3 RGB interface characteristics

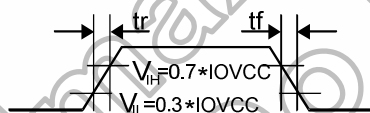


(VSSA=0V, IOVCC=1.65V to 3.3V, VCI=2.3V to 3.3V, Ta = -30 to 70° C)

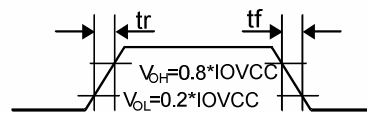
| Item   | Symbol             | Condition | Spec. |      |      | Unit   |
|--|--------------------|-----------|-------|------|------|--------|
|  |                    |           | Min.  | Typ. | Max. |        |
| Pixel low pulse width                        | T <sub>CLKLT</sub> | -         | 15    | -    | -    | ns     |
| Pixel high pulse width                       | T <sub>CLKHT</sub> | -         | 15    | -    | -    | ns     |
| Vertical Sync. set-up time                   | T <sub>VSST</sub>  | -         | 15    | -    | -    | ns     |
| Vertical Sync. hold time                     | T <sub>VSHT</sub>  | -         | 15    | -    | -    | ns     |
| Horizontal Sync. set-up time                 | T <sub>HSST</sub>  | -         | 15    | -    | -    | ns     |
| Horizontal Sync. hold time                   | T <sub>HSHT</sub>  | -         | 15    | -    | -    | ns     |
| Data Enable set-up time                      | T <sub>DEST</sub>  | -         | 15    | -    | -    | ns     |
| Data Enable hold time                        | T <sub>DEHT</sub>  | -         | 15    | -    | -    | ns     |
| Data set-up time                             | T <sub>DST</sub>   | -         | 15    | -    | -    | ns     |
| Data hold time                               | T <sub>DHT</sub>   | -         | 15    | -    | -    | ns     |
| Phase difference of sync signal falling edge | Thv                | -         | 0     | -    | 240  | Dotclk |

**Note:** The input signal rise time and fall time (tr, tf) is specified at 15 ns or less.

Input Signal Slope

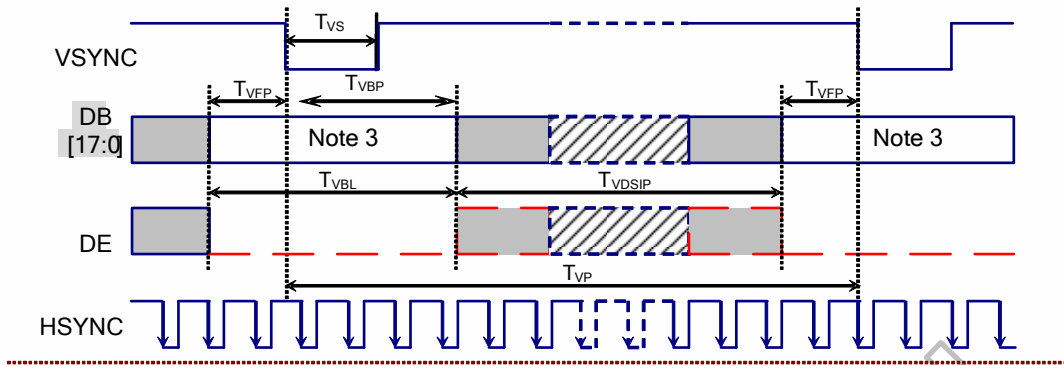


Output Signal Slope

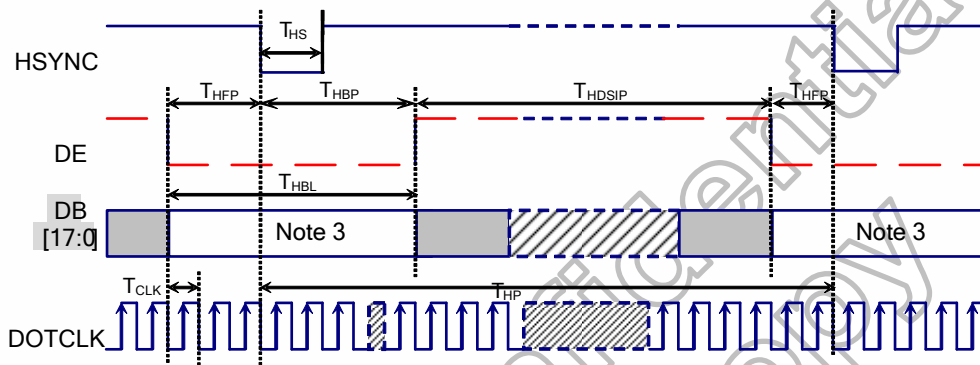




Vertical Timing for RGB I/F



Horizontal Timing for RGB I/F



| Item                       | Symbol       | Condition           | Spec. |      |      | Unit   |
|----------------------------|--------------|---------------------|-------|------|------|--------|
|                            |              |                     | Min.  | Typ. | Max. |        |
| <b>Vertical Timing</b>     |              |                     |       |      |      |        |
| Vertical cycle period      | $T_{VP}$     | -                   | 324   | 326  | 452  | HS     |
| Vertical low pulse width   | $T_{VS}$     | -                   | 2     | 2    | -    | HS     |
| Vertical front porch       | $T_{VFP}$    | -                   | 2     | 2    | 6    | HS     |
| Vertical back porch        | $T_{VBP}$    | -                   | 2     | 4    | 126  | HS     |
| Vertical blanking period   | $T_{VBL}$    | $T_{VBP} + T_{VFP}$ | 4     | 6    | 132  | HS     |
| Vertical active area       | $T_{VDISP}$  | -                   | -     | 320  | -    | HS     |
|                            |              |                     | -     |      | -    | HS     |
|                            |              |                     | -     |      | -    | HS     |
| Vertical refresh rate      | TVRR         | Frame rate          | 50    | 60   | 80   | Hz     |
| <b>Horizontal Timing</b>   |              |                     |       |      |      |        |
| Horizontal cycle period    | $T_{HP}$     | -                   | 244   | 252  | 1008 | DOTCLK |
| Horizontal low pulse width | $T_{HS}$     | -                   | 2     | 2    | 256  | DOTCLK |
| Horizontal front porch     | $T_{HFP}$    | -                   | 2     | 4    | 256  | DOTCLK |
| Horizontal back porch      | $T_{HBP}$    | -                   | 2     | 8    | 256  | DOTCLK |
| Horizontal blanking period | $T_{HBL}$    | $T_{HBP} + T_{HFP}$ | 4     | 12   | 256  | DOTCLK |
| Horizontal active area     | $T_{HDISP}$  | -                   | -     | 240  | -    | DOTCLK |
| Pixel clock cycle          | $f_{CLKCYC}$ | -                   | 3.9   | -    | 16.6 | MHz    |
| TVRR=60Hz                  |              |                     |       |      |      |        |

**Note:** (1) IOVCC=1.65 to 3.3V, VCI=2.3 to 3.3V, VSSA=VSSD=0V,  $T_A$ =-30 to 70°C (to +85°C no damage)

(2) Data lines can be set to "High" or "Low" during blanking time – Don't care.

(3) HP is multiples of DOTCLK.

(4) 16.6MHz is using at below condition: 324(Hs)x1008(DOTCLK)x50(Hz)

### 8.5.4 Reset input timing

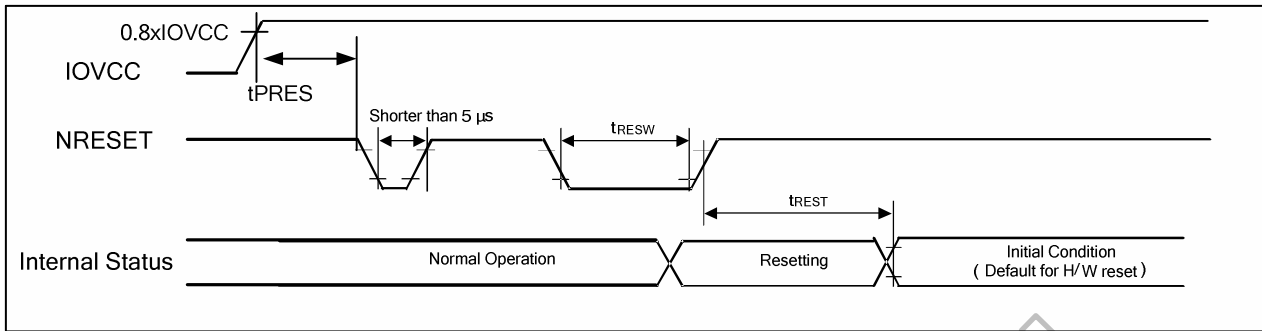


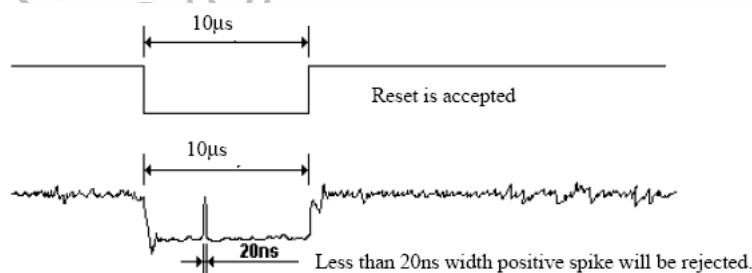
Figure 8.5: Reset input timing

| Symbol | Parameter                                 | Related Pins   | Spec. |      |      | Note                                   | Unit |
|--------|---|----------------|-------|------|------|--|------|
|        |   |                | Min.  | Typ. | Max. |  |      |
| tRESW  | Reset low pulse width <sup>(1)</sup>      | NRESET         | 10    | -    | -    | -                                      | μs   |
| tREST  | Reset complete time <sup>(2)</sup>        | -              | 5     | -    | -    | When reset applied during STB OUT mode | ms   |
|        |   | -              | 120   | -    | -    | When reset applied during STB mode     | ms   |
| tPRES  | Reset goes high level after Power on time | NRESET & IOVCC | 1     | -    | -    | Reset goes high level after Power on   | ms   |

**Note:** (1) Spike due to an electrostatic discharge on NRESET line does not cause irregular system reset according to the table below.

| NRESET Pulse           | Action         |
|------------------------|----------------|
| Shorter than 5 μs      | Reset Rejected |
| Longer than 10 μs      | Reset          |
| Between 5 μs and 10 μs | Reset Start    |

- (2) During the resetting period, the display will be blanked (The display is entering blanking sequence, which maximum time is 120 ms, when Reset Starts in STB Out –mode. The display remains the blank state in STB –mode) and then return to Default condition for H/W reset.
- (3) During Reset Complete Time, VMF value in OTP will be latched to internal register during this period. This loading is done every time when there is H/W reset complete time (tREST) within 5ms after a rising edge of NRESET.
- (4) Spike Rejection also applies during a valid reset pulse as shown below:



- (5) It is necessary to wait 5msec after releasing !RES before sending commands. Also STB Out

## 9. Ordering Information

| Part No.                 | Package   |
|--------------------------|---|
| HX8347-G000 <u>PDxxx</u> | PD : mean COG<br>xxx : mean chip thickness ( $\mu\text{m}$ ), (default: 250 $\mu\text{m}$ ) |

## 10. Revision History

| Version | Date       | Description of Changes   |
|---------|------------|--|
| 01      | 2009/09/09 | New setup  |
|         | 2009/10/15 | 1. P17~P19: modify Pin Description.<br>2. P29: add serial interface II.                            |
|         | 2009/11/18 | 1. P19 modify Pin assignment 250 $\mu\text{m}$<br>2. P63 GRAM X address and display panel position |
|         | 2009/12/03 | 1. P14 modify VCI operation range.   |
|         | 2010/01/25 | 1.P178 modify twc description  |
|         | 2010/02/03 | 1. P178 modify tRCFM description   |
|         | 2010/07/15 | 1. P18: modify Pin Description of VCOM_DUMMY   |

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